DAQ

NI 6013/6014 User Manual

Multifunction I/O Devices for PCI Bus Computers

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Compliance

FCC/Canada Radio Frequency Interference Compliance

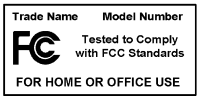
Determining FCC Class

The Federal Communications Commission (FCC) has rules to protect wireless communications from interference. The FCC places digital electronics into two classes. These classes are known as Class A (for use in industrial-commercial locations only) or Class B (for use in residential or commercial locations). Depending on where it is operated, this product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.)

Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products. By examining the product you purchased, you can determine the FCC Class and therefore which of the two FCC/DOC Warnings apply in the following sections. (Some products may not be labeled at all for FCC; if so, the reader should then assume these are Class A devices.)

FCC Class A products only display a simple warning statement of one paragraph in length regarding interference and undesired operation. Most of our products are FCC Class A. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

FCC Class B products display either a FCC ID code, starting with the letters **EXN**, or the FCC Class B compliance mark that appears as shown here on the right.



Consult the FCC Web site at `http://www.fcc.gov` for more information.

FCC/DOC Warnings

This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual and the CE Marking Declaration of Conformity*, may cause interference to radio and television reception. Classification requirements are the same for the Federal Communications Commission (FCC) and the Canadian Department of Communications (DOC).

Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.

Class A

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Class B

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Canadian Department of Communications

This Class B digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe B respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Compliance to EU Directives

Readers in the European Union (EU) must refer to the Manufacturer's Declaration of Conformity (DoC) for information* pertaining to the CE Marking compliance scheme. The Manufacturer includes a DoC for most every hardware product except for those bought for OEMs, if also available from an original manufacturer that also markets in the EU, or where compliance is not required as for electrically benign apparatus or cables.

To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

* The CE Marking Declaration of Conformity will contain important supplementary information and instructions for the user or installer.

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About This Manual

The National Instruments 6013/6014 devices are high-performance multifunction analog, digital, and timing I/O devices for PCI. The NI 6014 features 16 channels (eight differential) of 16-bit analog input (AI), two channels of 16-bit analog output (AO), a 68-pin connector, and eight lines of digital I/O (DIO). The NI 6013 is identical to the NI 6014, except that it does not have AO channels.

This manual describes the electrical and mechanical aspects of the NI 6013/6014 and contains information concerning their operation and programming.

Conventions Used in This Manual

The following conventions are used in this manual:

<> — Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DIO<3..0>. Angle brackets can also denote a variable in a channel name—for example, ACH<*i*> and ACH<*i*+8>.

♦ — The ♦ symbol indicates that the text following it applies only to a specific product, a specific operating system, or a specific software version.

» — The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

— This icon denotes a note, which alerts you to important information.

— This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the device, refer to Appendix A, *Specifications*, for precautions to take.

6013/6014 — This phrase denotes the NI PCI-6013 and NI PCI-6014 devices.

bold — Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names and hardware labels.

italic	Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.
`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.
NI-DAQ	NI-DAQ refers to the NI-DAQ driver software for PC compatible computers unless otherwise noted.
PC	PC refers to all PC AT series computers with PCI bus unless otherwise noted.

Related Documentation

The following documents contain information you may find helpful:

- *DAQ Quick Start Guide*, at `ni.com/manuals`
- *DAQ-STC Technical Reference Manual*, at `ni.com/manuals`
- NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals*, at `ni.com/zone`
- *NI-DAQ User Manual for PC Compatibles*, at `ni.com/manuals`
- *PCI Local Bus Specification Revision 2.3*, at `pcisig.com`

1 Introduction

This chapter describes the NI 6013/6014, lists what you need to get started, describes the optional software and equipment, and explains how to unpack the NI 6013/6014.

About the NI 6013/6014 Device

Thank you for buying an NI 6013/6014. The NI 6014 features 16 channels (eight differential) of 16-bit analog input, two channels of 16-bit analog output, a 68-pin connector, and eight lines of digital I/O. The NI 6013 is identical to the NI 6014, except that it does not have AO channels.

The NI 6013/6014 uses the NI data acquisition system timing controller (DAQ-STC) for time-related functions. The DAQ-STC consists of three timing groups that control AI, AO, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns. The DAQ-STC makes possible such applications as buffered pulse generation, equivalent time sampling, and seamless changing of the sampling rate.

What You Need to Get Started

To set up and use the device, you need the following items:

- ❑ At least one of the following devices:
  - NI 6013 for PCI
  - NI 6014 for PCI
- ❑ *NI 6013/6014 User Manual*
- ❑ NI-DAQ (for PC Compatibles)

- ❑ One of the following software packages and documentation:
  - LabVIEW (for Windows)
  - Measurement Studio (for Windows)
  - VI Logger
- ❑ A PCI-bus computer

Software Programming Choices

When programming National Instruments DAQ hardware, you can use an NI application development environment (ADE) or other ADEs. In either case, you use NI-DAQ.

NI-DAQ

NI-DAQ, which ships with the NI 6013/6014, has an extensive library of functions that you can call from the ADE. These functions allow you to use all the features of the NI 6013/6014.

NI-DAQ carries out many of the complex interactions, such as programming interrupts, between the computer and the DAQ hardware. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to the code. Whether you are using LabVIEW, Measurement Studio, VI Logger, or other ADEs, your application uses NI-DAQ, as illustrated in Figure 1-1.

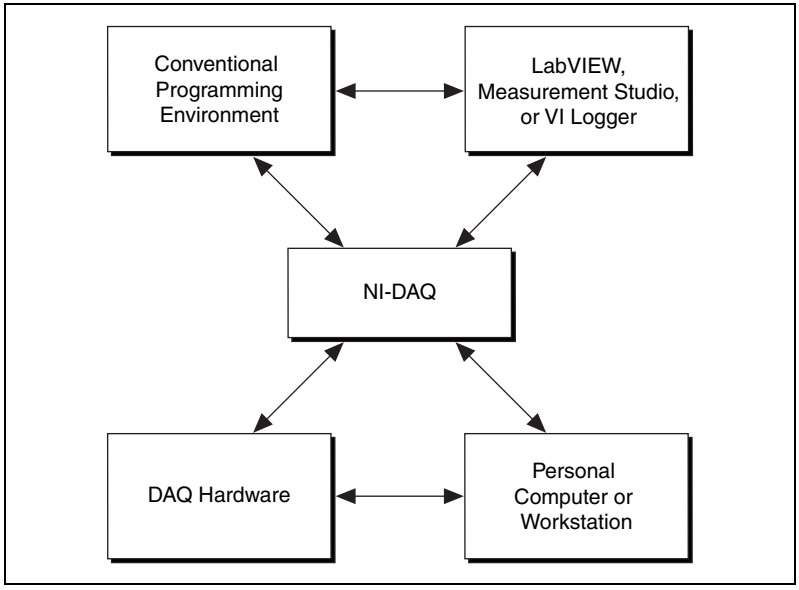


Figure 1-1. The Relationship Among the Programming Environment, NI-DAQ, and the Hardware

To download a free copy of the most recent version of NI-DAQ, click **Download Software** at `ni.com`.

National Instruments ADE Software

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

Measurement Studio, which includes LabWindows™/CVI™, tools for Visual C++, and tools for Visual Basic, is a development suite that allows you to use ANSI C, Visual C++, and Visual Basic to design the test and measurement software. For C developers, Measurement Studio includes LabWindows/CVI, a fully integrated ANSI C application development environment that features interactive graphics and the LabWindows/CVI Data Acquisition and Easy I/O libraries. For Visual Basic developers, Measurement Studio features a set of ActiveX controls for using National Instruments DAQ hardware. These ActiveX controls provide a high-level programming interface for building virtual instruments. For Visual C++ developers, Measurement Studio offers a set of Visual C++ classes and tools to integrate those classes into Visual C++ applications. The libraries,

ActiveX controls, and classes are available with Measurement Studio and NI-DAQ.

Using LabVIEW, Measurement Studio, or VI Logger greatly reduces the development time for your data acquisition and control application.

Optional Equipment

NI offers a variety of products to use with the device, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded screw terminals
- Low channel-count signal conditioning modules, devices, and accessories, including conditioning for strain gauges and resistance temperature detectors (RTDs), simultaneous sample and hold, and relays

For more information about these products, refer to the NI catalog at `ni.com/catalog`.

Unpacking

The NI 6013/6014 is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge (ESD) can damage several components on the device.

Caution *Never* touch the exposed pins of connectors.

To avoid such damage in handling the device, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the device from the package.

Remove the device from the package and inspect the device for loose components or any sign of damage. Notify NI if the device appears damaged in any way. Do *not* install a damaged device into the computer.

Store the NI 6013/6014 in the antistatic envelope when not in use.

Safety Information

The following section contains important safety information that you *must* follow during installation and use of the product.

Do *not* operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to NI for repair.

If the product is rated for use with hazardous voltages (>30 V_{rms}, 42.4 V_{pk}, or 60 V_{DC}), you may need to connect a safety earth-ground wire according to the installation instructions. Refer to Appendix A, *Specifications*, for maximum voltage ratings.

Do *not* substitute parts or modify the product. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the product.

Do *not* operate the product in an explosive atmosphere or where there may be flammable gases or fumes. Operate the product only at or below the pollution degree stated in Appendix A, *Specifications*. Pollution is foreign matter in a solid, liquid, or gaseous state that can produce a reduction of dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution Degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution Degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution Degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs, which becomes conductive due to condensation.

Clean the product with a soft nonmetallic brush. The product *must* be completely dry and free from contaminants before returning it to service.

You *must* insulate signal connections for the maximum voltage for which the product is rated. Do *not* exceed the maximum ratings for the product. Remove power from signal lines before connection to or disconnection from the product.

Operate this product only at or below the installation category stated in Appendix A, *Specifications*.

The following is a description of installation categories:

- Installation Category I is for measurements performed on circuits not directly connected to MAINS[1]. This category is a signal level such as voltages on a printed wire board (PWB) on the secondary of an isolation transformer.

  Examples of Installation Category I are measurements on circuits not derived from MAINS and specially protected (internal) MAINS-derived circuits.

- Installation Category II is for measurements performed on circuits directly connected to the low-voltage installation. This category refers to local-level distribution such as that provided by a standard wall outlet.

  Examples of Installation Category II are measurements on household appliances, portable tools, and similar equipment.

- Installation Category III is for measurements performed in the building installation. This category is a distribution level referring to hardwired equipment that does not rely on standard building insulation.

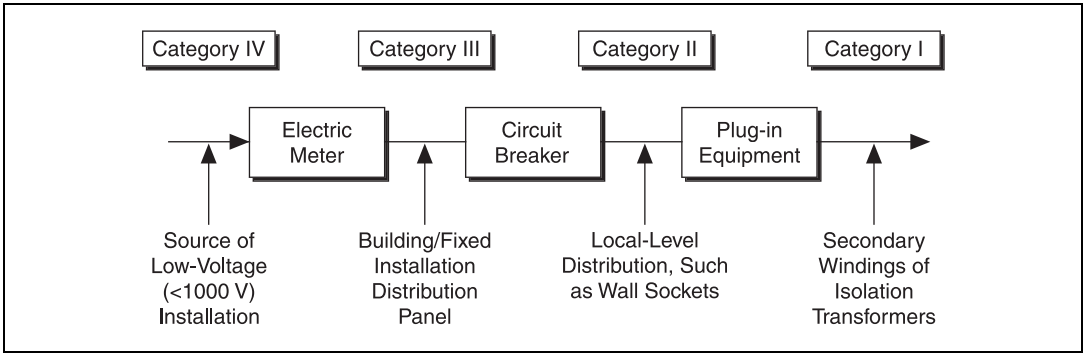
  Examples of Installation Category III include measurements on distribution circuits and circuit breakers. Other examples of Installation Category III are wiring including cables, bus-bars, junction boxes, switches, socket outlets in the building/fixed installation, and equipment for industrial use, such as stationary motors with a permanent connection to the building/fixed installation.

- Installation Category IV is for measurements performed at the source of the low-voltage (<1,000 V) installation.

  Examples of Installation Category IV are electric meters, and measurements on primary overcurrent protection devices and ripple-control units.

[1] MAINS is defined as the electricity supply system to which the equipment concerned is designed to be connected either for powering the equipment or for measurement purposes.

Below is a diagram of a sample installation.



2

Installing and Configuring the NI 6013/6014

This chapter explains how to install and configure the NI 6013/6014.

Installing the Software

Complete the following steps to install the software before installing the NI 6013/6014.

1. Install the ADE, such as LabVIEW, Measurement Studio, or VI Logger, according to the instructions on the CD and the release notes.
2. Install NI-DAQ according to the instructions on the CD and the *DAQ Quick Start Guide* included with the NI 6013/6014.

Note It is important to install NI-DAQ before installing the NI 6013/6014 to ensure that the NI 6013/6014 is properly detected.

Installing the Hardware

The NI 6013/6014 fits in any PCI system slot in the computer. However, to achieve best noise performance, leave as much room as possible between the NI 6013/6014 and other devices.

The following are general installation instructions, but consult the computer user manual or technical reference manual for specific instructions and warnings.

Note Follow the guidelines in the computer documentation for installing plug-in hardware.

1. Power off and unplug the computer.
2. Remove the cover.

3. Make sure there are no lighted LEDs on the motherboard. If any are lit, wait until they go out before continuing the installation.
4. Remove the expansion slot cover on the back panel of the computer.
5. Ground yourself using a grounding strap or by holding a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of Chapter 1, *Introduction*.
6. Insert the NI 6013/6014 into a PCI system slot. Gently rock the device to ease it into place. It may be a tight fit, but do *not* force the device into place.
7. If required, screw the mounting bracket of the device to the back panel rail of the computer.
8. Visually verify the installation. Make sure the device is not touching other devices or components and is fully inserted into the slot.
9. Replace the cover.
10. Plug in and power on the computer.

Note For proper cooling, all covers and filler panels must be installed when operating the device.

The NI 6013/6014 is now installed. You are now ready to configure the device.

Configuring the Hardware

Because of the NI standard architecture for data acquisition and standard bus specifications, the NI 6013/6014 is completely software configurable. Two types of configuration are performed on the NI 6013/6014: bus-related and data acquisition-related.

The NI 6013/6014 device is fully compatible with the industry-standard *PCI Local Bus Specification Revision 2.3*. This specification allows the PCI system to automatically perform all bus-related configurations with no user interaction. Bus-related configuration includes setting the device base memory address and interrupt channel.

Data acquisition-related configuration, which you must perform, includes such settings as AI coupling and range, and others. You can modify these settings using NI-DAQ or ADE software, such as LabVIEW and Measurement Studio. Refer to the software documentation for configuration instructions. Refer to Chapter 3, *Hardware Overview*, for more information about the various settings available for the device.

To configure the NI 6013/6014 in Measurement & Automation Explorer (MAX), refer to `ni.com/manuals` to view either the *DAQ Quick Start Guide* or the *NI-DAQ User Manual for PC Compatibles*, or launch MAX to access the Measurement & Automation Explorer Help for DAQ (**Help»Help Topics»NI-DAQ**).

3

Hardware Overview

This chapter presents an overview of the hardware functions on the NI 6013/6014.

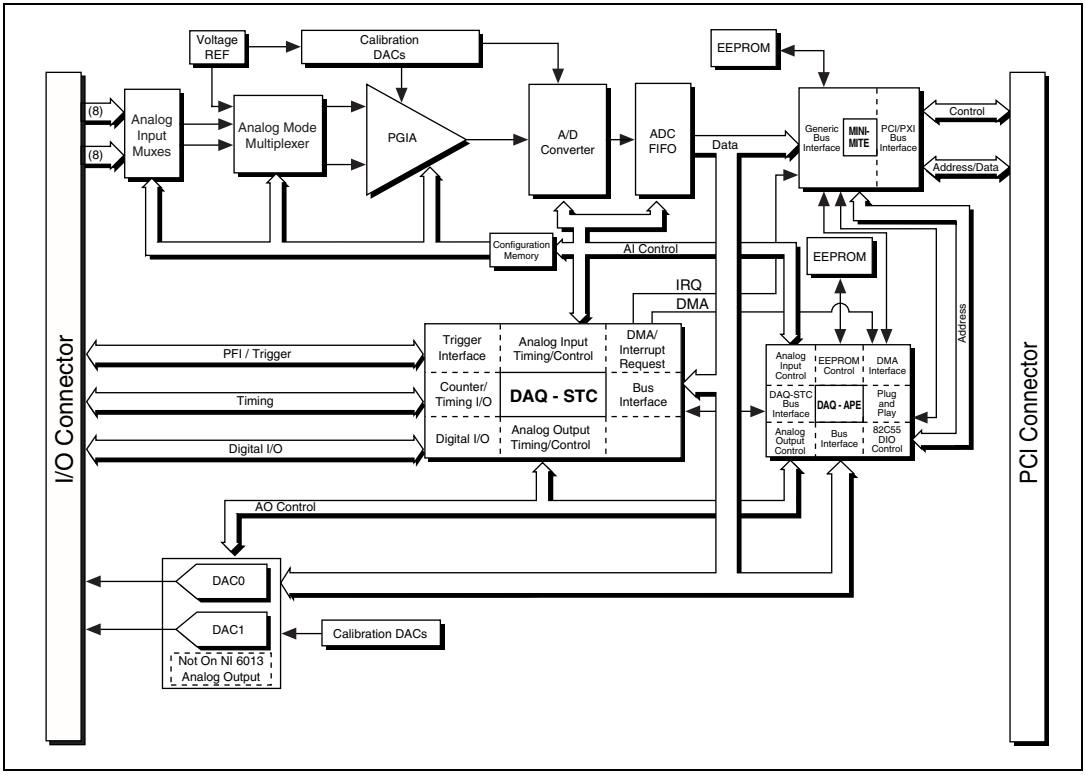


Figure 3-1. NI 6013/6014 Block Diagram

Analog Input

The AI section of the NI 6013/6014 is software configurable. The following sections describe in detail each AI setting.

Input Mode

The NI 6013/6014 has two input modes—nonreferenced single-ended (NRSE) mode and differential (DIFF) mode. NRSE mode provides up to 16 channels. DIFF input mode provides up to eight channels. Input modes are programmed on a per channel basis for multimode scanning. For example, you can configure the circuitry to scan 12 channels—four differentially configured channels and eight single-ended channels. Table 3-1 describes the two input modes.

Table 3-1. Available Input Modes

Mode	Description
DIFF	A channel configured in DIFF mode uses two AI lines. One line connects to the positive input of the programmable gain instrumentation amplifier (PGIA) on the device, and the other connects to the negative input of the PGIA.
NRSE	A channel configured in NRSE mode uses one AI line, which connects to the positive input of the PGIA. The negative input of the PGIA connects to AI sense (AISENSE).

For diagrams showing the signal paths of the two configurations, refer to the *Connecting Analog Input Signals* section of Chapter 4, *Connecting Signals*.

Input Range

The NI 6013/6014 has a bipolar input range that changes with the programmed gain. Each channel may be programmed with a unique gain of 0.5, 1.0, 10, or 100 to maximize the A/D converter (ADC) resolution. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-2 shows the input range and precision according to the gain used.

Table 3-2. Measurement Precision

Gain	Input Range	Precision[1]
0.5	–10 to +10 V	305.2 µV
1.0	–5 to +5 V	152.6 µV
10.0	–500 to +500 mV	15.3 µV
100.0	–50 to +50 mV	1.53 µV

[1] The value of 1 least significant bit (LSB) of the 16-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 16-bit count.

Note: Refer to Appendix A, *Specifications*, for absolute maximum ratings.

Scanning Multiple Channels

The devices can scan multiple channels at the same maximum rate as their single-channel rate; however, pay careful attention to the settling times for each device. No extra settling time is necessary between channels as long as the gain is constant and source impedances are low. Refer to Appendix A, *Specifications*, for a complete listing of settling times for each of the devices.

When scanning among channels at various gains, the settling times may increase. When the PGIA switches to a higher gain, the signal on the previous channel may be well outside the new, smaller range. For instance, suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1, and suppose the PGIA is programmed to apply a gain of one to channel 0 and a gain of 100 to channel 1. When the multiplexer switches to channel 1 and the PGIA switches to a gain of 100, the new full-scale range is ±50 mV.

The approximately 4 V step from 4 V to 1 mV is 4,000% of the new full-scale range. It may take as long as 100 µs for the circuitry to settle to 1 LSB after such a large transition. In general, this extra settling time is not needed when the PGIA is switching to a lower gain.

Settling times can also increase when scanning high-impedance signals because of a phenomenon called *charge injection*, where the AI multiplexer injects a small amount of charge into each signal source when that source is selected. If the impedance of the source is not low enough, the effect of the charge—a voltage error—does not decay by the time the ADC samples the signal. For this reason, keep source impedances under 1 kΩ to perform high-speed scanning.

Due to the previously described limitations of settling times resulting from these conditions, multiple-channel scanning is not recommended unless sampling rates are low enough or it is necessary to sample several signals as nearly simultaneously as possible. The data is much more accurate and channel-to-channel independent if you acquire data from each channel independently (for example, 100 points from channel 0, then 100 points from channel 1, then 100 points from channel 2, and so on.)

Analog Output

- NI 6014 only

The NI 6014 supplies two channels of 16-bit AO voltage at the I/O connector. Each device has a fixed bipolar output range of ±10 V. Data written to the D/A converter (DAC) is interpreted in two's complement format, where for a number x expressed in base 2 with n digits to the left of the radix point, the (base 2) number is $2n - x$.

Analog Output Glitch

In normal operation, a DAC output glitches whenever it is updated with a new value. The glitch energy differs from code to code and appears as distortion in the frequency spectrum.

Digital I/O

The NI 6013/6014 contains eight lines of digital I/O (DIO<0..7>) for general-purpose use. You can individually software-configure each line for either input or output. At system startup and reset, the DIO ports are all high-impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the general-purpose counters. The up/down

control signals, GPCTR0_UP_DOWN and GPCTR1_UP_DOWN, are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC chip provides a flexible interface for connecting timing signals to other devices or external circuitry. The NI 6013/6014 uses the Programmable Function Input (PFI) pins on the I/O connector to connect the device to external circuitry. These connections are designed to enable the NI 6013/6014 to both control and be controlled by other devices and circuits.

The DAQ-STC has 13 internal timing signals that can be controlled by an external source. These timing signals can also be controlled by signals generated internally to the DAQ-STC, and these selections are fully software configurable. Figure 3-2 shows an example of the signal routing multiplexer controlling the CONVERT* signal.

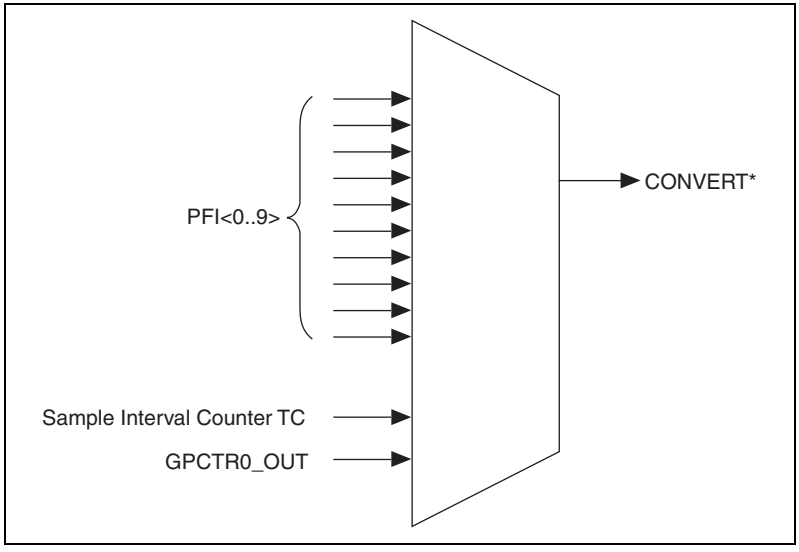


Figure 3-2. CONVERT* Signal Routing

Figure 3-2 shows that CONVERT* can be generated from a number of sources, including the external signals PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Many of these timing signals are also available on the PFI pins, as indicated in Chapter 4, *Connecting Signals*.

Programmable Function Inputs

The 10 PFI pins are connected to the signal routing multiplexer for each timing signal, and software can select any PFI pin as the external source for a given timing signal. It is important to note that any of the PFI pins can be used as an input by any of the timing signals and that multiple timing signals can simultaneously use the same PFI. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications.

To use the PFI pins as outputs, you must use the Route Signal VI or the Select Signal VI to individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software must turn on the output driver for the PFI5/UPDATE* pin.

4

Connecting Signals

This chapter describes how to make input and output signal connections to the NI 6013/6014 using the I/O connector. Table 4-1 shows the cables that can be used with the I/O connectors to connect to different accessories.

Table 4-1. I/O Connector Details

Device with I/O Connector	Number of Pins	Cable for Connecting to 100-pin Accessories	Cable for Connecting to 68-pin Accessories	Cable for Connecting to 50-pin Signal Accessories
PCI-6013/6014	68	N/A	SH6868 Shielded Cable, SH68-68R1-EP Shielded Cable, R6868 Ribbon Cable	SH6850 Shielded Cable, R6850 Ribbon Cable

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI 6013/6014 can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections. The *Protection* column of Table 4-3 shows the maximum input ratings for each signal.

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector. Refer to Appendix B, *Custom Cabling and Optional Connectors*, for pin assignments of the optional 50- and 68-pin connectors. A signal description follows the figures.

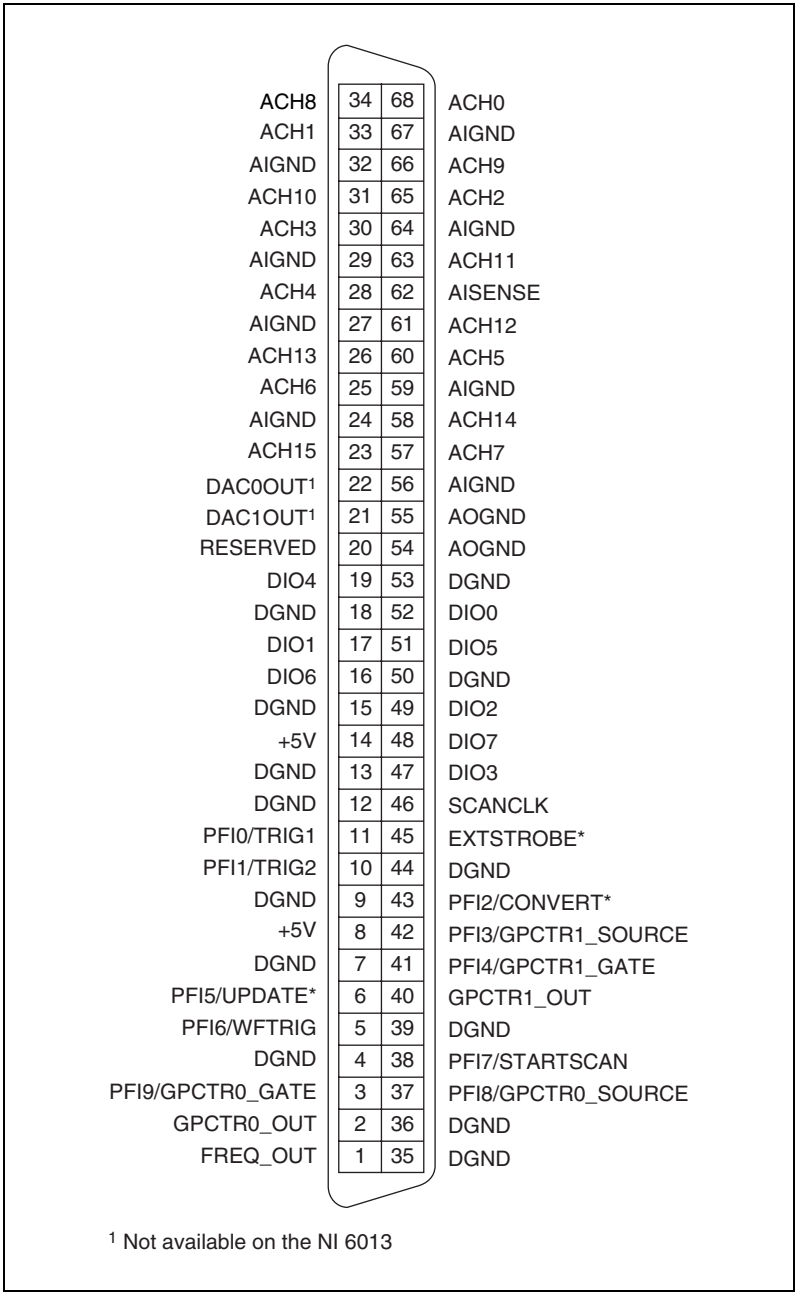

ACH8 34 68 ACH0
ACH1 33 67 AIGND
AIGND 32 66 ACH9
ACH10 31 65 ACH2
ACH3 30 64 AIGND
AIGND 29 63 ACH11
ACH4 28 62 AISENSE
AIGND 27 61 ACH12
ACH13 26 60 ACH5
ACH6 25 59 AIGND
AIGND 24 58 ACH14
ACH15 23 57 ACH7
DAC0OUT1 22 56 AIGND
DAC1OUT1 21 55 AOGND
RESERVED 20 54 AOGND
DIO4 19 53 DGND
DGND 18 52 DIO0
DIO1 17 51 DIO5
DIO6 16 50 DGND
DGND 15 49 DIO2
+5V 14 48 DIO7
DGND 13 47 DIO3
DGND 12 46 SCANCLK
PFI0/TRIG1 11 45 EXTSTROBE*
PFI1/TRIG2 10 44 DGND
DGND 9 43 PFI2/CONVERT*
+5V 8 42 PFI3/GPCTR1_SOURCE
DGND 7 41 PFI4/GPCTR1_GATE
PFI5/UPDATE* 6 40 GPCTR1_OUT
PFI6/WFTRIG 5 39 DGND
DGND 4 38 PFI7/STARTSCAN
PFI9/GPCTR0_GATE 3 37 PFI8/GPCTR0_SOURCE
GPCTR0_OUT 2 36 DGND
FREQ_OUT 1 35 DGND
1 Not available on the NI 6013

Figure 4-1. I/O Connector Pin Assignment for the NI 6013/6014

Table 4-2. Signal Descriptions for I/O Connector Pins

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog Input Ground—These pins are the bias current return point for AI measurements. Refer to Figure 4-3 for recommended connections. All three ground references—AIGND, AOGND, and DGND—are connected on the device.
ACH<0..15>	AIGND	Input	Analog Input Channels 0 through 15—Each channel pair, ACH<*i*, *i*+8> (*i* = 0..7), can be configured as either one differential input or two single-ended inputs.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for any of channels ACH<0..15> in NRSE configuration. AISENSE must be connected to AIGND directly or to an external ground reference for single-ended measurements. Invalid random readings result if AISENSE is left unconnected when using NRSE mode. Refer to Figure 4-3 for recommended connections.
DAC0OUT[1]	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of AO channel 0.
DAC1OUT[1]	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of AO channel 1.
AOGND	—	—	Analog Output Ground—The AO voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected on the device.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply. All three ground references—AIGND, AOGND, and DGND—are connected together on the device.
DIO<0..7>	DGND	Input Output	Digital I/O Signals—DIO6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
+5V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-resetting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion in scanning mode when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.

Table 4-2. Signal Descriptions for I/O Connector Pins (Continued)

Signal Name	Reference	Direction	Description
PFI0/TRIG1	DGND	Input Output	PFI0/Trigger 1—As an input, this signal is a Programmable PFI. PFI signals are explained in the *Connecting Timing Signals* section. As an output, this signal is the TRIG1 (AI Start Trigger) signal. In posttriggered DAQ sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretriggered applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input Output	PFI1/Trigger 2—As an input, this signal is a PFI. As an output, this signal is the TRIG2 (AI Stop Trigger) signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.
PFI2/CONVERT*	DGND	Input Output	PFI2/Convert—As an input, this signal is a PFI. As an output, this signal is the CONVERT* (AI Convert) signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input Output	PFI3/Counter 1 Source—As an input, this signal is a PFI. As an output, this signal is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input Output	PFI4/Counter 1 Gate—As an input, this signal is a PFI. As an output, this signal is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input Output	PFI5/Update—As an input, this signal is a PFI. As an output, this signal is the UPDATE* (AO Update) signal. A high-to-low edge on UPDATE* indicates that the AO primary group is being updated for the NI 6014.
PFI6/WFTRIG	DGND	Input Output	PFI6/Waveform Trigger—As an input, this signal is a PFI. As an output, this signal is the WFTRIG (AO Start Trigger) signal. In timed AO sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7/STARTSCAN	DGND	Input Output	PFI7/Start of Scan—As an input, this signal is a PFI. As an output, this signal is the STARTSCAN (AI Scan Start) signal. This pin pulses once at the start of each AI scan in the interval scan. A low-to-high transition indicates the start of the scan.

Table 4-2. Signal Descriptions for I/O Connector Pins (Continued)

Signal Name	Reference	Direction	Description
PFI8/GPCTR0_SOURCE	DGND	Input Output	PFI8/Counter 0 Source—As an input, this signal is a PFI. As an output, this signal is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input Output	PFI9/Counter 0 Gate—As an input, this signal is a PFI. As an output, this signal is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

* Indicates that the signal is active low.

[1] Not available on the NI 6013.

Table 4-3. I/O Signal Summary for the NI 6013/6014

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±200 pA
AISENSE	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±200 pA
AIGND	AO	—	—	—	—	—	—
DAC0OUT (NI 6014only)	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	4 V/µs	—
DAC1OUT (NI 6014 only)	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	4 V/µs	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
V_{CC}	DO	0.1 Ω	Short-circuit to ground	1A fused	—	—	—

Table 4-3. I/O Signal Summary for the NI 6013/6014 (Continued)

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
DIO<0..7>	DIO	—	V_{CC} +0.5	10 at (V_{CC} –0.4)	24 at 0.4	1.1	1.5 kΩ pd
SCANCLK	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI1/TRIG2	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu

pd = pull down
pu = pull up
DO = Digital Output

The tolerance on the 50 kΩ pull-up resistors is very large. Actual value may range between 17 and 100 kΩ.

Analog Input Signal Overview

The AI signals for the NI 6013/6014 are ACH<0..15>, AISENSE, and AIGND. Connection of these AI signals to the device depends on the type of input signal source and the configuration of the AI channels you are using. This section provides an overview of the different types of signal sources and AI configuration modes. More specific signal connection information is provided in the *Connecting Analog Input Signals* section.

Types of Signal Sources

When making signal connections, you must first determine whether the signal sources are floating or ground-referenced. The following sections describe these two types of signals.

Floating Signal Sources

A floating signal source is not connected in any way to the building ground system but, rather, has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must tie the ground reference of a floating signal to the NI 6013/6014 AIGND to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats outside the common-mode input range.

Ground-Referenced Signal Sources

A ground-referenced signal source is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the NI 6013/6014, assuming that the computer is plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV, but it can be much higher if power distribution circuits are improperly connected. If a grounded signal source is improperly measured, this difference may appear as a measurement error. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

Analog Input Modes

You can use the NI 6013/6014 PGIA in different ways, depending on whether you configure the NI 6013/6014 for NRSE or DIFF mode. Figure 4-2 shows a diagram of the device PGIA.

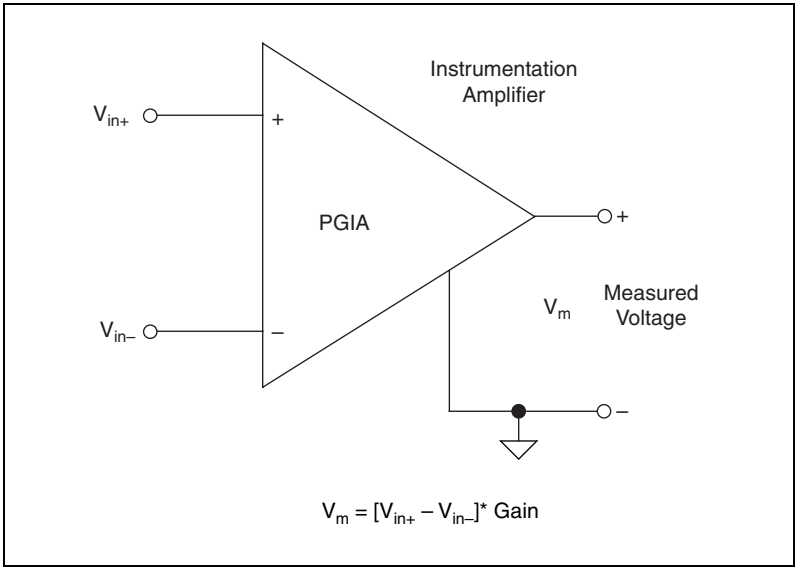


Figure 4-2. Programmable Gain Instrumentation Amplifier (PGIA)

In NRSE mode, signals connected to ACH<0..15> are routed to the positive input of the PGIA, and AISENSE is connected to the negative input of the PGIA. In DIFF mode, signals connected to ACH<0..7> are routed to the positive input of the PGIA, signals connected to ACH<8..15> are routed to the negative input of the PGIA, and AISENSE is not used.

Caution Exceeding the differential and common-mode input ranges distorts the input signals. Exceeding the maximum input voltage rating can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections. The maximum input voltage ratings are listed in the *Protection* column of Table 4-3.

AIGND is an AI common signal that is routed directly to the ground tie point on the devices. You can use this signal for a general analog ground tie point to the device if necessary.

Note AIGND is not connected to the negative input of the PGIA in single-ended mode unless it is connected to AISENSE with an external wire.

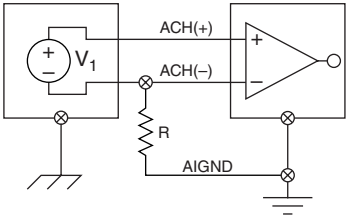
The PGIA applies gain and common-mode voltage rejection and presents high-input impedance to the AI signals connected to the device. Signals are routed to the positive and negative inputs of the PGIA through input multiplexers on the device. The PGIA converts two input signals to a signal that is the difference between the two input signals multiplied by the gain

setting of the amplifier. The amplifier output voltage is referenced to the device ground. The device ADC measures this output voltage when it performs A/D conversions.

Connecting Analog Input Signals

The following sections discuss the use of single-ended and differential measurements and make recommendations for measuring both floating and ground-referenced signal sources.

Figure 4-3 summarizes the recommended input configuration for both types of signal sources.

<table>
<tr><td rowspan="2">Input</td><td colspan="2">Input</td></tr>
<tr><td>Floating Signal Source
(Not Connected to Building Ground)</td><td>Grounded Signal Source</td></tr>
<tr><td></td><td>Examples
• Ungrounded Thermocouples
• Signal Conditioning with Isolated Outputs
• Battery Devices</td><td>Example
• Plug-in Instruments with Nonisolated Outputs</td></tr>
<tr><td>Differential (DIFF)</td><td> 

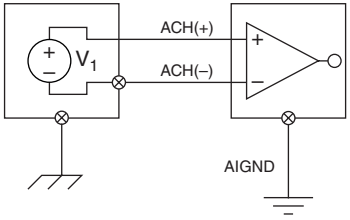
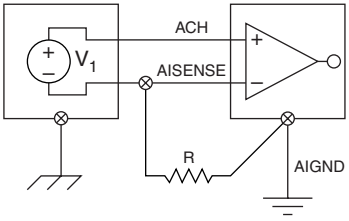
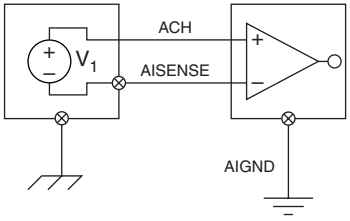
See text for information on bias resistors.</td><td> 
</td></tr>
<tr><td>Single-Ended — Nonreferenced (NRSE)</td><td> 
</td><td> 
</td></tr>
</table>

Figure 4-3. Summary of AI Connections

Differential Connection Considerations

A differential connection is one in which the AI signal has its own reference signal or signal return path. These connections are available when the selected channel is configured in DIFF input mode. In DIFF mode, the AI channels are paired, with ACH<*i*> as the signal input and ACH<*i*+8> as the signal reference. For example, ACH0 is paired with ACH8, ACH1 is paired with ACH9, and so on. The input signal is tied to the positive input of the PGIA, and its reference signal, or return, is tied to the negative input of the PGIA.

When you configure a channel for DIFF input mode, each signal uses two multiplexer inputs—one for the signal and one for its reference signal. Therefore, with a differential configuration for every channel, up to eight AI channels are available.

You should use DIFF input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the device are greater than 3 m (10 ft).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce noise pick up and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.

Differential Connections for Ground-Referenced Signal Sources

Figure 4-4 shows how to connect a ground-referenced signal source to a channel on the device configured in DIFF input mode.

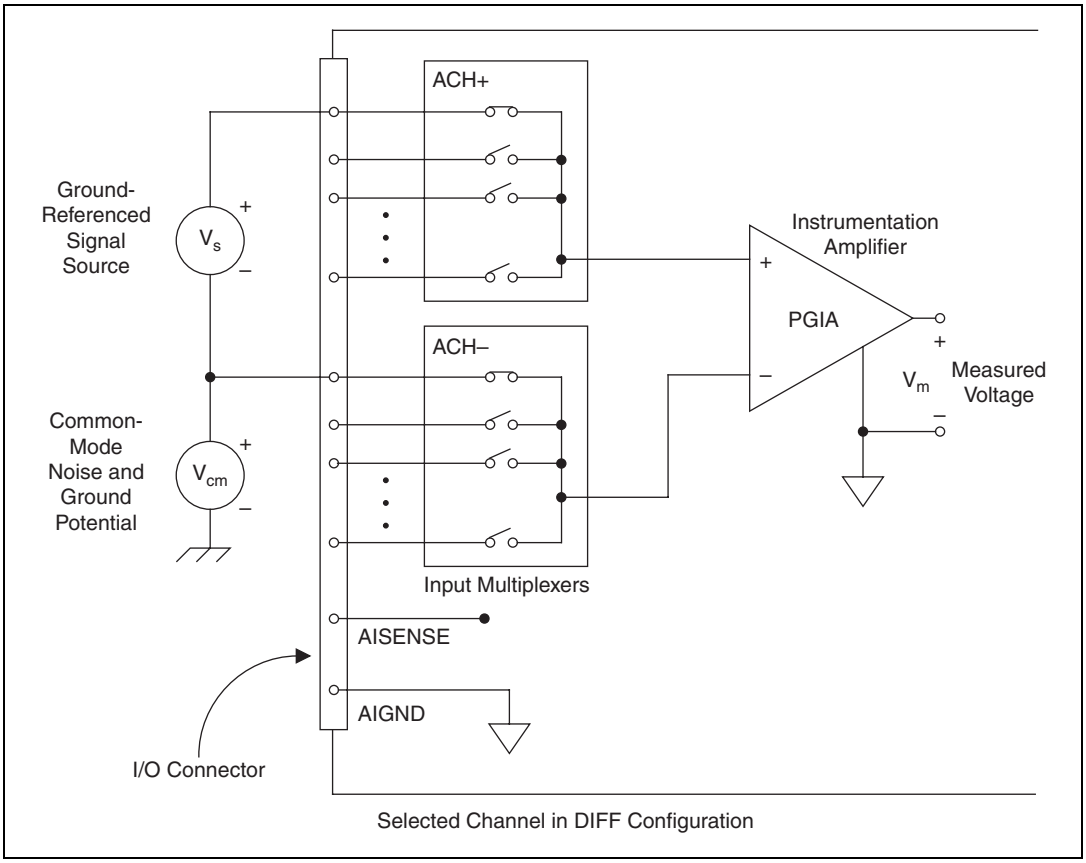


Figure 4-4. Differential Input Connections for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground, shown as V_{cm} in Figure 4-4.

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 4-5 shows how to connect a floating signal source to a channel configured in DIFF input mode on the NI 6013/6014.

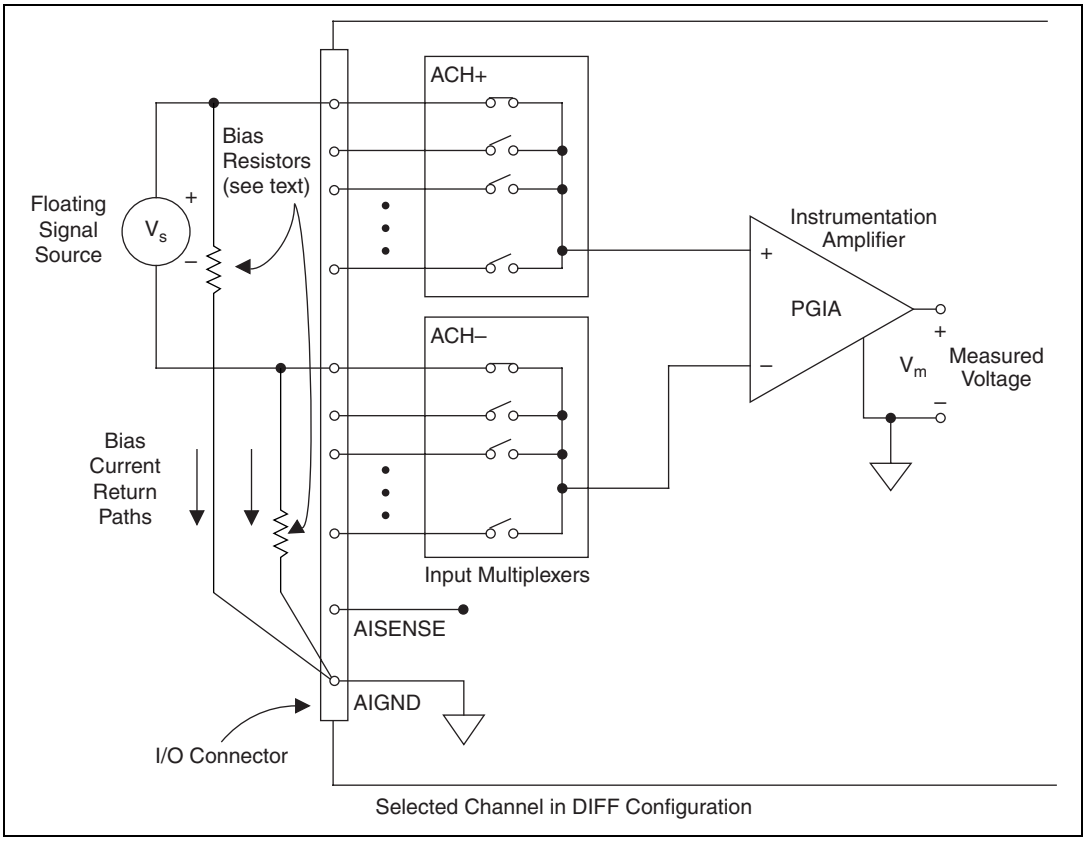


Figure 4-5. Differential Input Connections for Nonreferenced Signals

Figure 4-5 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is unlikely to remain within the common-mode signal range of the PGIA. The PGIA then saturates, causing erroneous readings.

You must reference the source to AIGND. The easiest way is to connect the positive side of the signal to the positive input of the PGIA and connect the negative side of the signal to AIGND as well as to the negative input of the PGIA, without any resistors. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

However, for larger source impedances, this connection leaves the differential signal path significantly off balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line, because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, and the PGIA does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically-coupled noise. Also, this configuration does not load down the source (other than the very high input impedance of the PGIA).

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 4-5. This fully balanced configuration offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the PGIA require a DC path to ground in order for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AIGND. If the source has low impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, you can tie the negative input directly to AIGND. If the source has high output impedance, you should balance the signal path as previously described using the same value resistor on both the positive and negative inputs. You should be aware that there is some gain error from loading down the source.

Single-Ended Connection Considerations

A single-ended connection is one in which the AI signal of the NI 6013/6014 is referenced to a common ground that can be shared with other input signals. The input signal is tied to the positive input of the PGIA, and the common ground is tied to the negative input of the PGIA using AISENSE.

When every channel is configured for single-ended input, up to 16 AI channels are available.

You can use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high level (greater than 1 V).
- The leads connecting the signal to the device are less than 3 m (10 ft).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

NRSE mode is the only single-ended configuration supported on the NI 6013/6014. The AISENSE connection differs for floating and grounded signal sources. For floating signal sources, AISENSE is connected directly to AIGND, and the NI 6013/6014 provides the reference ground point for the external signal. For grounded signal sources, AISENSE is connected to the external signal reference ground, preventing current loops and measurement errors.

In single-ended configurations, more electrostatic and magnetic noise couples into the signal connections than in differential configurations. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

Single-Ended Connections for Floating Signal Sources

Figure 4-6 shows how to connect a floating signal source to a channel configured for NRSE mode on the NI 6013/6014.

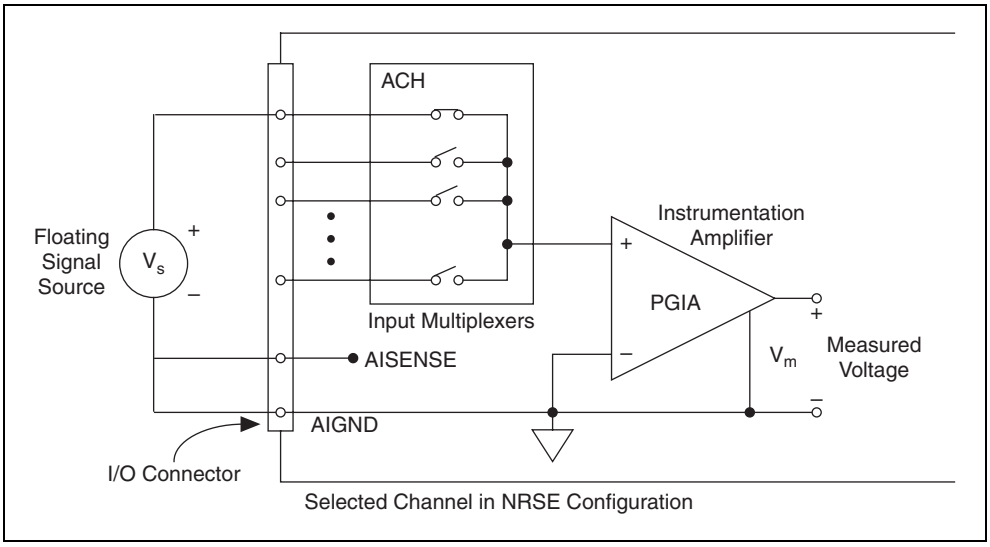


Figure 4-6. Single-Ended Input Connections for Nonreferenced or Floating Signals

Single-Ended Connections for Grounded Signal Sources

To measure a grounded signal source with a single-ended configuration, you must configure the NI 6013/6014 in NRSE input mode. The signal is then connected to the positive input of the PGIA, and the signal local ground reference is connected to the negative input of the PGIA. The ground point of the signal should, therefore, be connected to the AISENSE pin. Any potential difference between the device ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the PGIA, and this difference is rejected by the amplifier. If AISENSE is connected to AIGND in this situation, the difference in ground potentials appears as an error in the measured voltage.

Figure 4-7 shows how to connect a grounded signal source to a channel configured for NRSE mode on the NI 6013/6014.

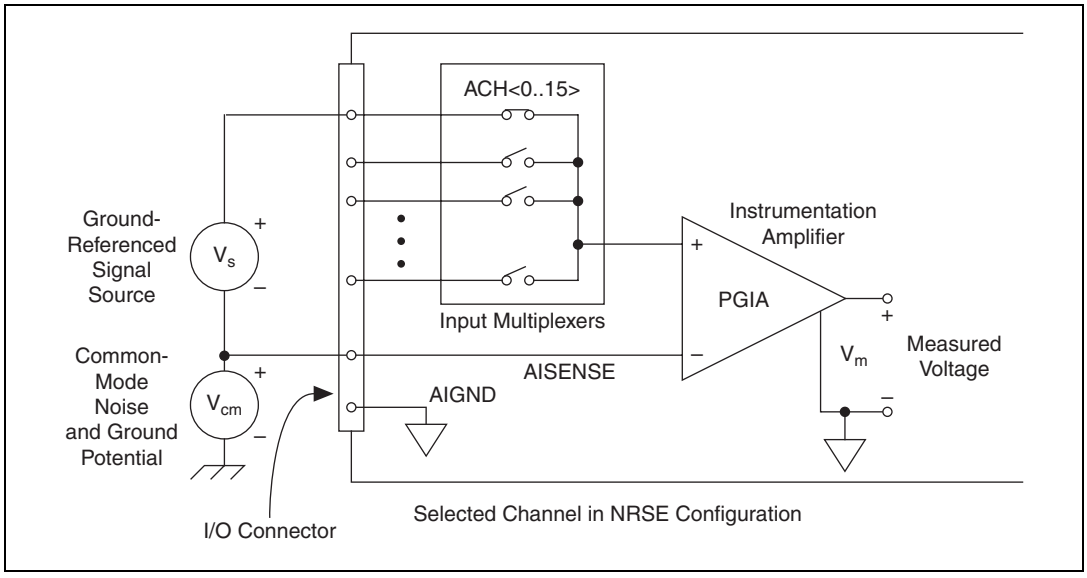


Figure 4-7. Single-Ended Input Connections for Ground-Referenced Signals

Common-Mode Signal Rejection Considerations

Figures 4-4 and 4-7 show connections for signal sources that are already referenced to some ground point with respect to the NI 6013/6014. In these cases, the PGIA can reject any voltage caused by ground potential differences between the signal source and the device. In addition, with differential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the device. The PGIA can reject common-mode signals as long as $V_{in}+$ and $V_{in}-$ (input signals) are both within ±11 V of AIGND.

Connecting Analog Output Signals

- NI 6014 only

The AO signals are DAC0OUT, DAC1OUT, and AOGND. DAC0OUT and DAC1OUT are not available on the NI 6013.

DAC0OUT is the voltage output signal for AO channel 0. DAC1OUT is the voltage output signal for AO channel 1.

AOGND is the ground-referenced signal for both AO channels and the external reference signal.

Figure 4-8 shows how to connect AO signals to the NI 6013/6014.

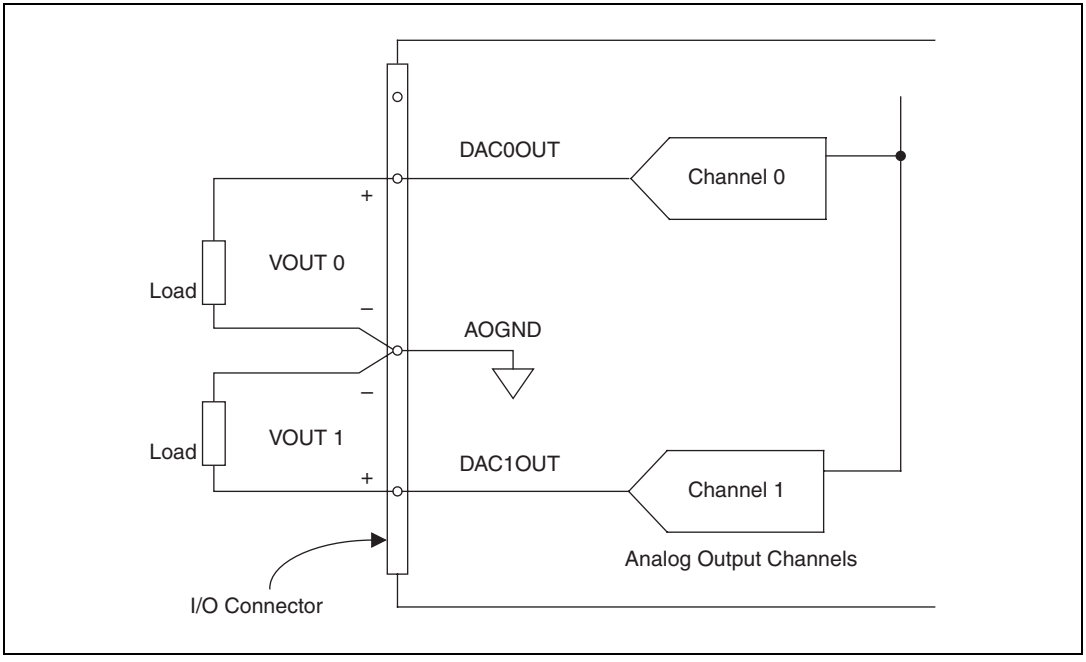


Figure 4-8. AO Connections

Connecting Digital I/O Signals

The DIO signals on the NI 6013/6014 are DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground-reference signal for the DIO port. You can program all lines individually to be inputs or outputs.

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-3, can damage the NI 6013/6014 and the computer. NI is *not* liable for any damage resulting from such signal connections.

Figure 4-9 shows signal connections for three typical DIO applications.

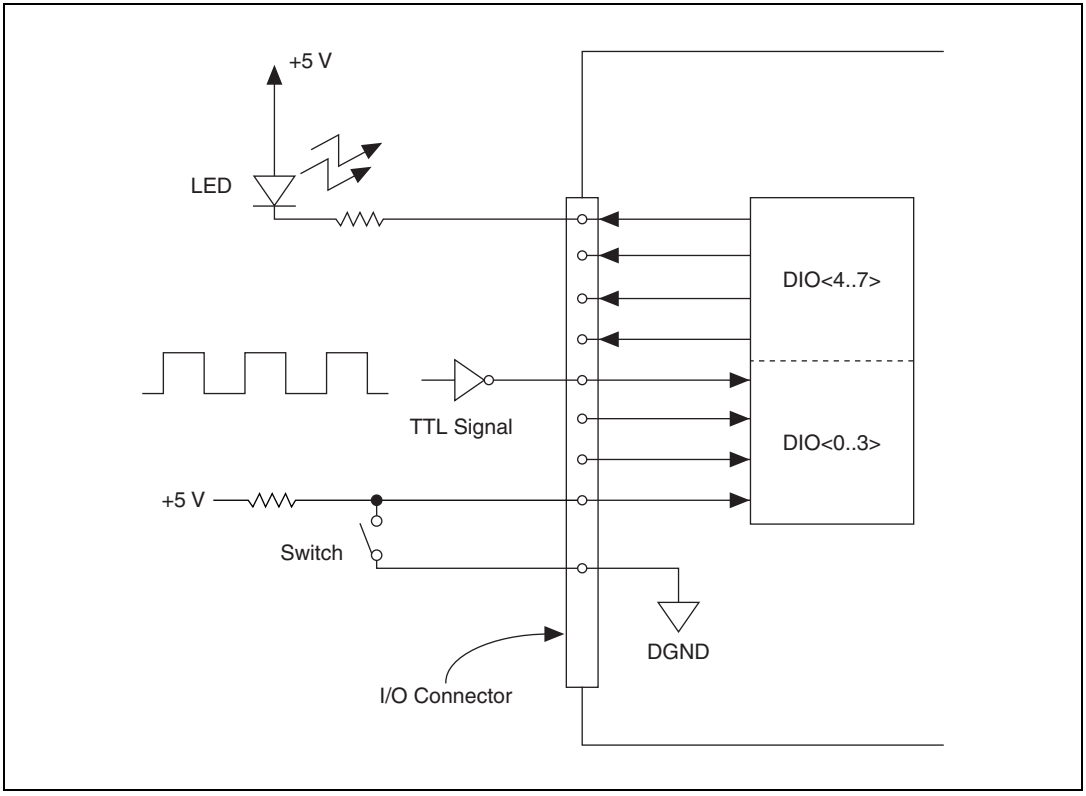


Figure 4-9. Digital I/O Connections

Figure 4-9 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states, such as the switch state shown in the Figure 4-9. Digital output applications include sending TTL signals and driving external devices, such as the LED shown in Figure 4-9.

Power Connections

Two pins on the I/O connector supply +5 V from the computer power supply using a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry. The power rating is +4.65 to +5.25 VDC at 1 A.

Caution Do *not* connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the NI 6013/6014 or any other device. Doing so can damage the NI 6013/6014 and the computer. NI is *not* liable for damage resulting from such a connection.

Connecting Timing Signals

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-3, can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections.

All external control over the timing of the device is routed through the 10 PFIs labeled PFI<0..9>. These signals are explained in detail in the *Programmable Function Input Connections* section. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many DAQ, waveform generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control any DAQ, waveform generation, and general-purpose timing signals.

The DAQ signals are explained in the *DAQ Timing Connections* section. The *Waveform Generation Timing Connections* section explains the waveform generation signals, and the *General-Purpose Timing Signal Connections* section explains the general-purpose timing signals.

All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-10, which shows how to connect an external TRIG1 source and an external CONVERT* source to two PFI pins on the NI 6013/6014.

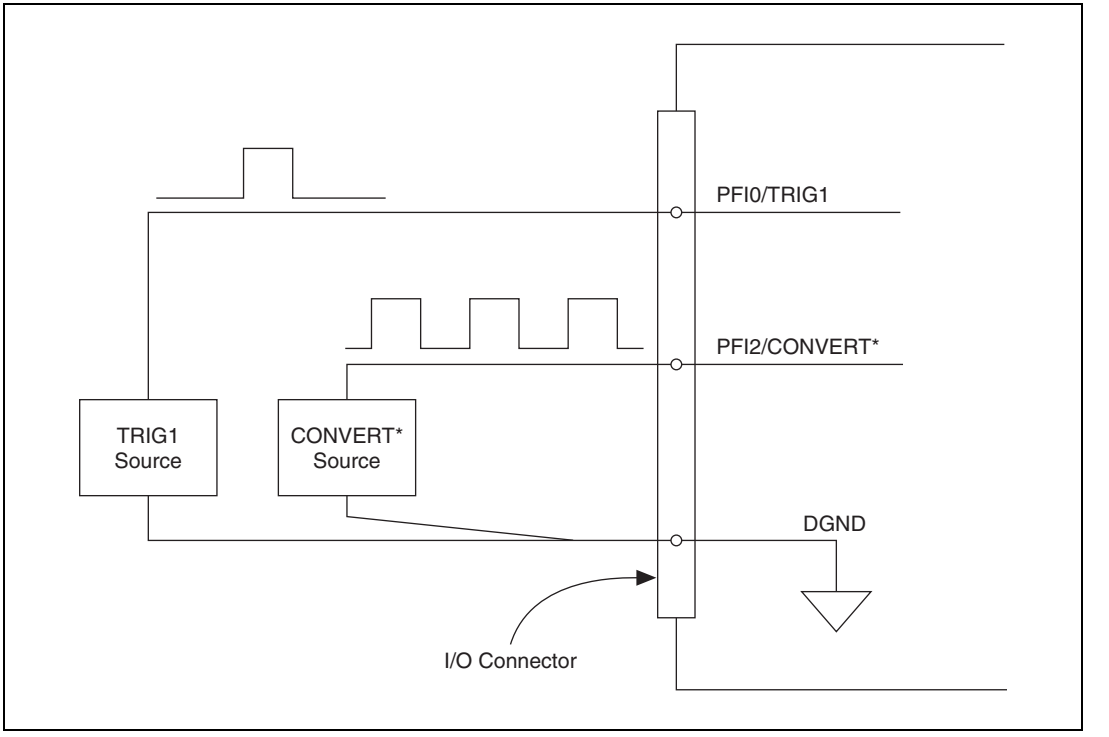


Figure 4-10. Timing I/O Connections

Programmable Function Input Connections

There are 13 internal timing signals that you can externally control from the PFI pins. The source for each of these signals is software-selectable from any PFI pin when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for different applications requiring alternative wiring.

You can individually enable each PFI pin to output a specific internal timing signal. For example, if you need the CONVERT* signal as an output on the I/O connector, software can turn on the output driver for the PFI2/CONVERT* pin.

Note Be careful not to drive a PFI signal externally when it is configured as an output.

As an input, each PFI pin can be individually configured for edge or level detection and for polarity selection. You can use the polarity selection for any of the timing signals, but the edge or level detection depends upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that individual signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse-width requirement in edge-detect mode.

In level-detection mode, there are no minimum or maximum pulse-width requirements imposed by the PFIs themselves, but there may be limits imposed by the particular timing signal being controlled. These requirements are listed later in this chapter.

DAQ Timing Connections

The DAQ timing signals are TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, SISOURCE, SCANCLK, and EXTSTROBE*.

Posttriggered data acquisition allows you to view only data that is acquired after a trigger event is received. A typical posttriggered DAQ sequence is shown in Figure 4-11.

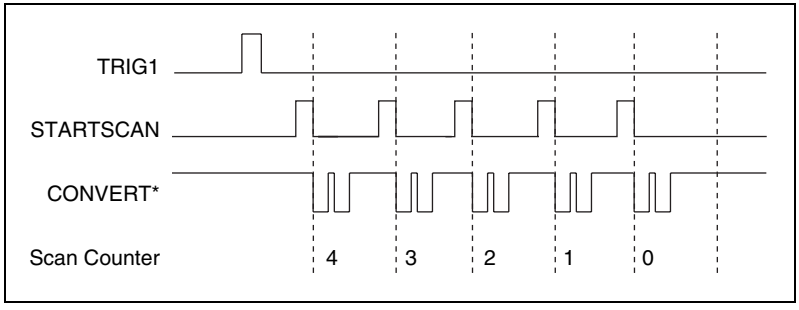


Figure 4-11. Typical Posttriggered Acquisition

Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-12 shows a typical pretriggered DAQ sequence. The description for each signal shown in these figures is included later in this chapter.

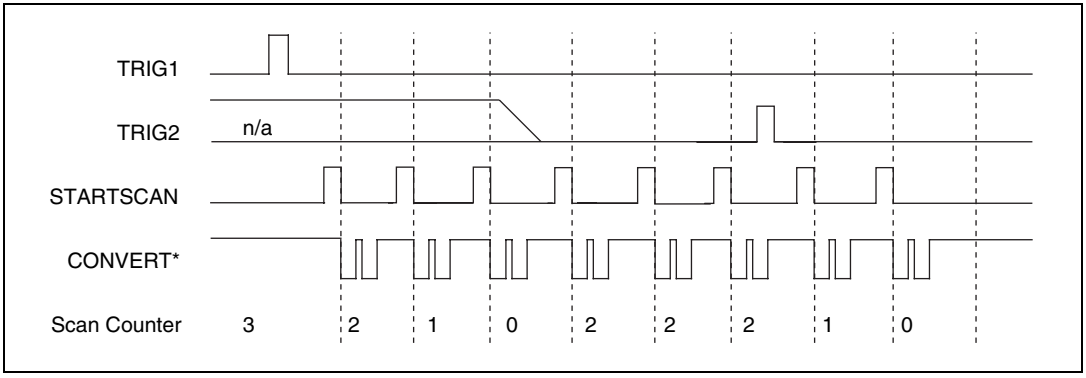


Figure 4-12. Typical Pretriggered Acquisition

TRIG1 Signal

Any PFI pin can externally input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin.

Refer to Figures 4-11 and 4-12 for the relationship of TRIG1 to the DAQ sequence.

As an input, TRIG1 is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of TRIG1 starts the DAQ sequence for both posttriggered and pretriggered acquisitions.

As an output, TRIG1 reflects the action that initiates a DAQ sequence, even if the acquisition is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-13 and 4-14 show the input and output timing requirements for TRIG1.

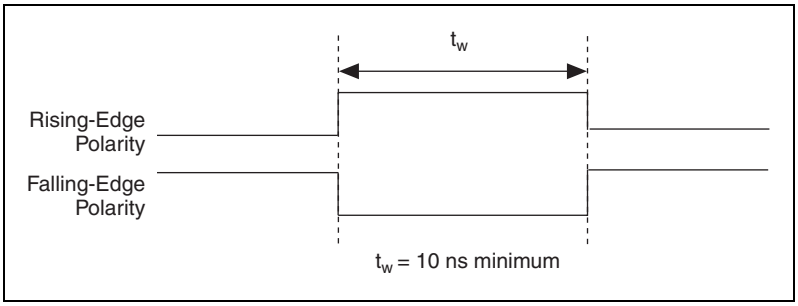


Figure 4-13. TRIG1 Input Signal Timing

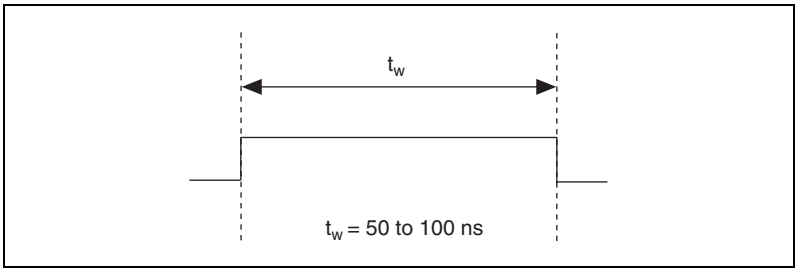


Figure 4-14. TRIG1 Output Signal Timing

The device also uses TRIG1 to initiate pretriggered DAQ operations. In most pretriggered applications, TRIG1 is generated by a software trigger. Refer to the TRIG2 signal description for a complete description of the use of TRIG1 and TRIG2 in a pretriggered DAQ operation.

TRIG2 Signal

Any PFI pin can externally input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin. Refer to Figure 4-12 for the relationship of TRIG2 to the DAQ sequence.

As an input, TRIG2 is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge of TRIG2 initiates the posttriggered phase of a pretriggered DAQ sequence. In pretriggered mode, the TRIG1 signal initiates the data acquisition. The scan counter (SC) indicates the minimum number of scans before TRIG2 can be recognized. After the SC decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The device

ignores TRIG2 if it is asserted prior to the SC decrementing to zero. After the selected edge of TRIG2 is received, the device acquires a fixed number of scans and the acquisition stops. This mode acquires data both before and after receiving TRIG2.

As an output, TRIG2 reflects the posttrigger in a pretriggered DAQ sequence, even if the acquisition is being externally triggered by another PFI. TRIG2 is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-15 and 4-16 show the input and output timing requirements for TRIG2.

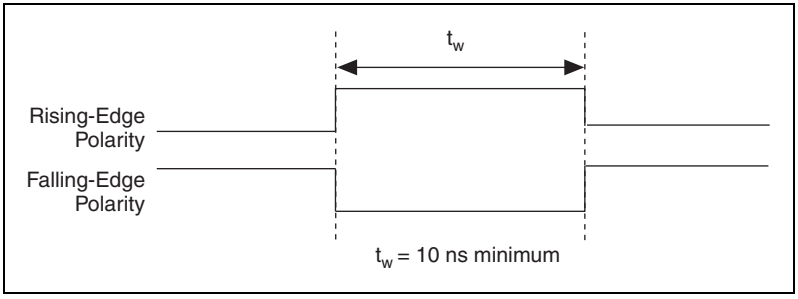


Figure 4-15. TRIG2 Input Signal Timing

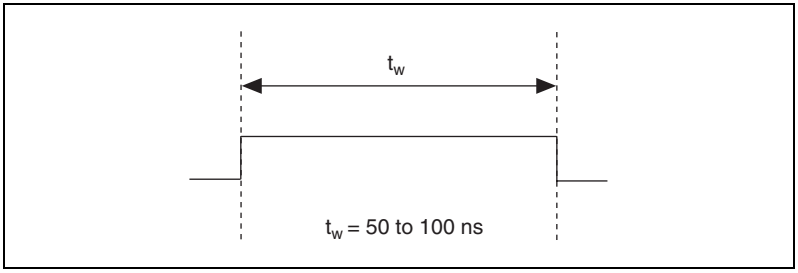


Figure 4-16. TRIG2 Output Signal Timing

STARTSCAN Signal

Any PFI pin can receive as an input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin. Refer to Figures 4-11 and 4-12 for the relationship of STARTSCAN to the DAQ sequence.

As an input, STARTSCAN is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of STARTSCAN initiates a scan. The sample interval counter starts if you select internally triggered CONVERT*.

As an output, STARTSCAN reflects the actual start pulse that initiates a scan, even if the starts are being externally triggered by another PFI. You have two output options. The first is an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the scan. The second action is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN is deasserted t_{off} after the last conversion in the scan is initiated. This output is set to high-impedance at startup.

Figures 4-17 and 4-18 show the input and output timing requirements for the STARTSCAN signal.

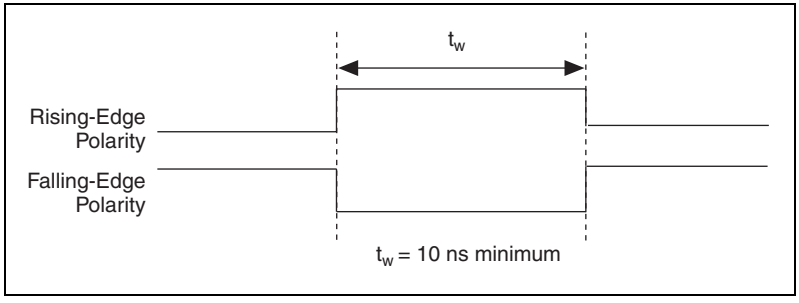


Figure 4-17. STARTSCAN Input Signal Timing

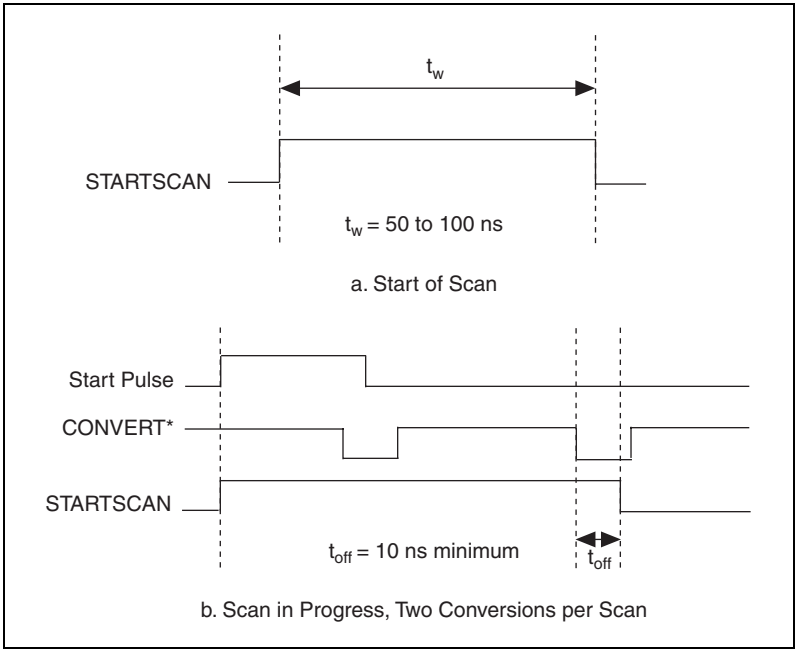


Figure 4-18. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the device generates the STARTSCAN signal. If you are using internally generated conversions, the first CONVERT* appears when the onboard sample interval counter (SI2) reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN generates a conversion. The STARTSCAN pulses should be separated by at least one scan period.

A counter on the NI 6013/6014 internally generates STARTSCAN unless you select some external source. This counter is started by the TRIG1 signal and is stopped either by software or by the sample counter.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

CONVERT* Signal

Any PFI pin can externally input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-11 and 4-12 for the relationship of CONVERT* to the DAQ sequence.

As an input, CONVERT* is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of CONVERT* initiates an A/D conversion.

The ADC switches to hold mode within 60 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next. CONVERT* pulses should be separated by at least 5 µs (200 kHz sample rate).

As an output, CONVERT* reflects the actual convert pulse that is connected to the ADC, even if the conversions are being externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 150 ns. This output is set to high-impedance at startup.

Figures 4-19 and 4-20 show the input and output timing requirements for CONVERT*.

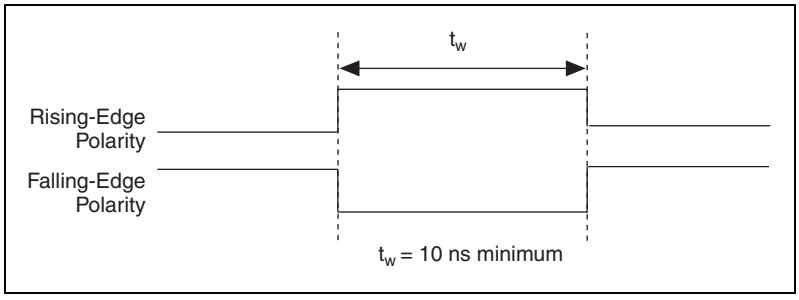


Figure 4-19. CONVERT* Input Signal Timing

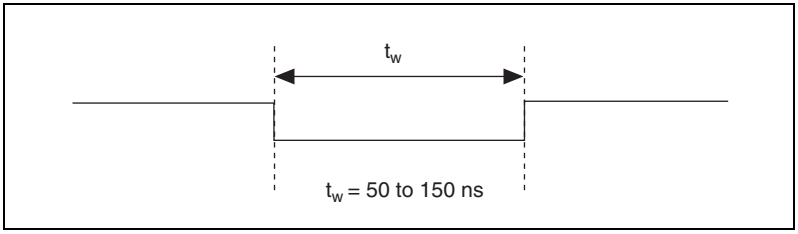


Figure 4-20. CONVERT* Output Signal Timing

The SI2 counter on the NI 6013/6014 normally generates CONVERT* unless you select some external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan is finished. It then reloads itself in preparation for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

AIGATE Signal

Any PFI pin can externally input the AIGATE signal, which is not available as an output on the I/O connector. AIGATE can mask off scans in a DAQ sequence. You can configure the PFI pin you select as the source for AIGATE in level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low. In level-detection mode if AIGATE is active, the STARTSCAN signal is masked off and no scans can occur.

AIGATE can neither stop a scan in progress nor continue a previously gated-off scan; in other words, once a scan has started, AIGATE does not gate off conversions until the beginning of the next scan and, conversely, if conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can externally input the SISOURCE signal, which is not available as an output on the I/O connector. The onboard scan interval (SI) counter uses SISOURCE as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for SISOURCE in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase generates SISOURCE unless you select some external source. Figure 4-21 shows the timing requirements for the SISOURCE signal.

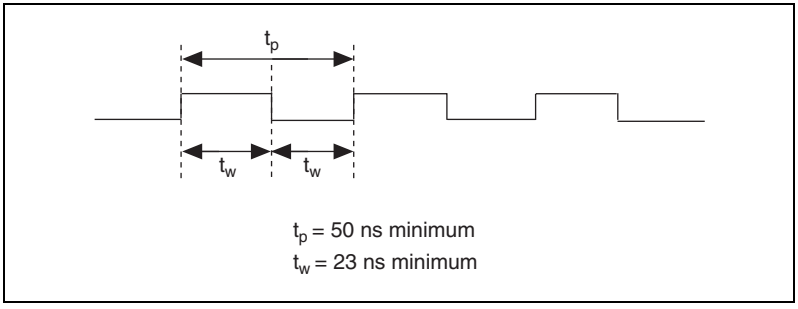


Figure 4-21. SISOURCE Signal Timing

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software-selectable but is typically configured so that a low-to-high leading edge can clock external AI multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software enabled.

Figure 4-22 shows the timing for SCANCLK.

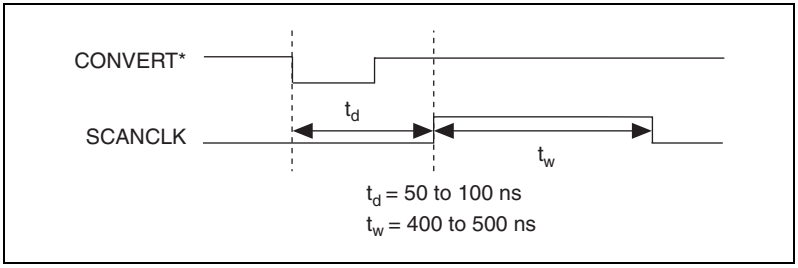


Figure 4-22. SCANCLK Signal Timing

Note When using NI-DAQ, SCANCLK polarity is low-to-high and cannot be changed programmatically.

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of EXTSTROBE*. A 10 µs and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode.

Figure 4-23 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

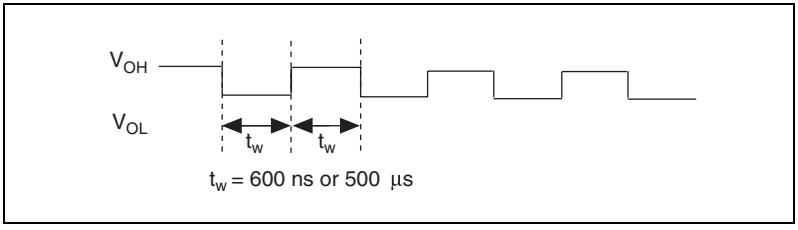


Figure 4-23. EXTSTROBE* Signal Timing

Note EXTSTROBE* cannot be enabled through NI-DAQ.

Waveform Generation Timing Connections

The analog group defined for the device is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, WFTRIG is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of WFTRIG starts the waveform generation for the DACs. The update interval (UI) counter is started if you select internally generated UPDATE*.

As an output, WFTRIG reflects the trigger that initiates waveform generation, even if the waveform generation is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-24 and 4-25 show the input and output timing requirements for WFTRIG.

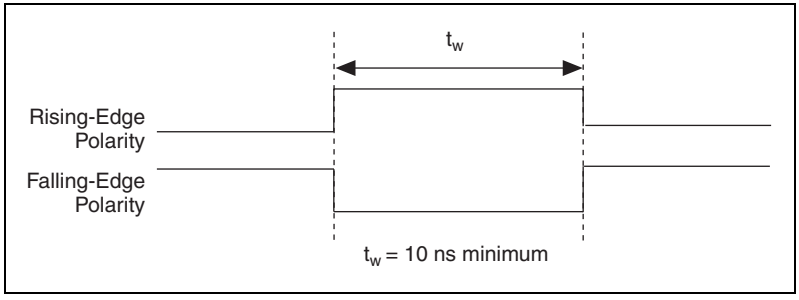


Figure 4-24. WFTRIG Input Signal Timing

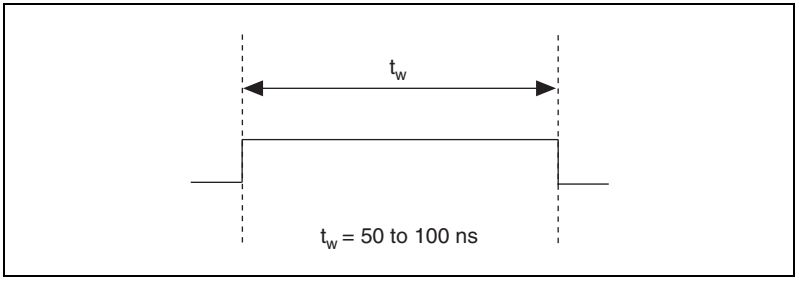


Figure 4-25. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, UPDATE* is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of UPDATE* updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, UPDATE* reflects the actual update pulse that is connected to the DACs, even if the updates are being externally generated by another PFI. The output is an active low pulse with a pulse width of 300 to 350 ns. This output is set to high-impedance at startup.

Figures 4-26 and 4-27 show the input and output timing requirements for UPDATE*.

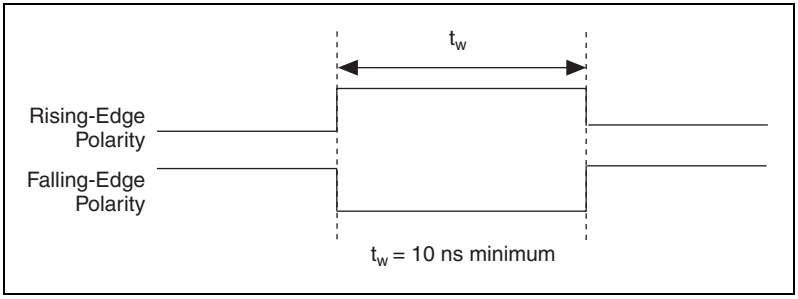


Figure 4-26. UPDATE* Input Signal Timing

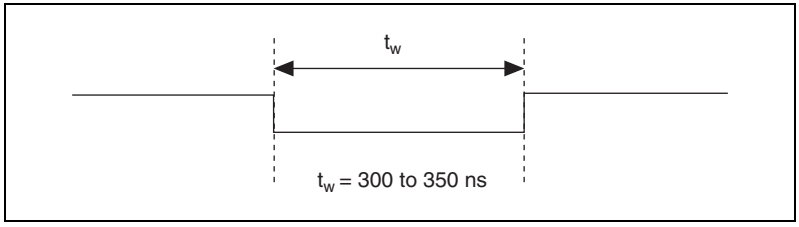


Figure 4-27. UPDATE* Output Signal Timing

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The device UI counter normally generates the UPDATE* signal unless you select some external source. The UI counter is started by the WFTRIG signal and can be stopped by software or the internal Buffer Counter (BC). D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. The UI counter uses UISOURCE as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for UISOURCE in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low. Figure 4-28 shows the timing requirements for UISOURCE.

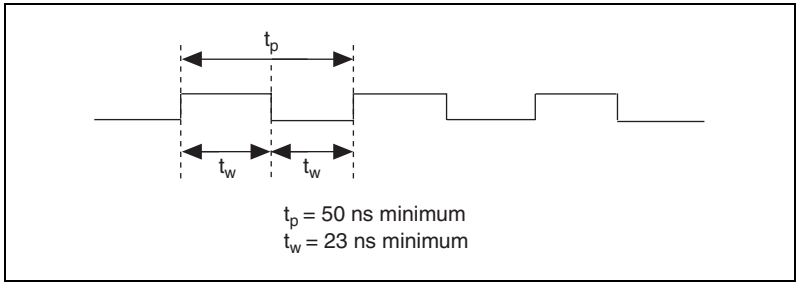


Figure 4-28. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase normally generates UISOURCE unless you select some external source.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, GPCTR0_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR0_SOURCE reflects the actual clock connected to general-purpose counter 0, even if another PFI externally inputs the source clock. This output is set to high-impedance at startup.

Figure 4-29 shows the timing requirements for GPCTR0_SOURCE.

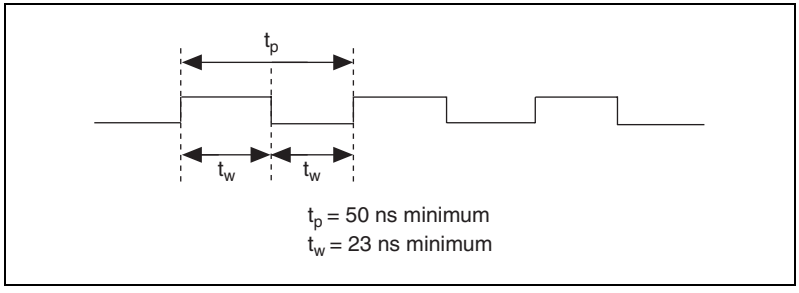


Figure 4-29. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates GPCTR0_SOURCE unless you select some external source.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, GPCTR0_GATE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform actions such as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, GPCTR0_GATE reflects the actual gate signal connected to general-purpose counter 0, even if the gate is being externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-30 shows the timing requirements for GPCTR0_GATE.

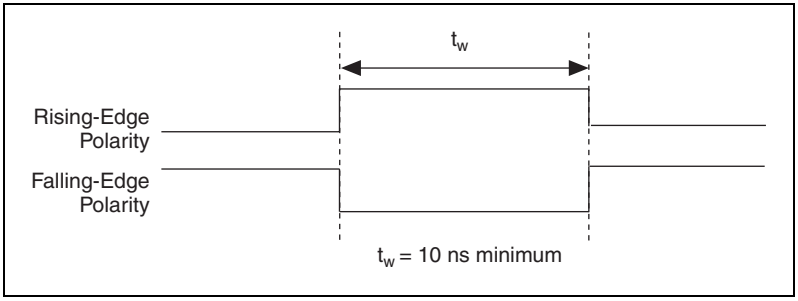


Figure 4-30. GPCTR0_GATE Signal Timing in Edge-Detection Mode

GPCTR0_OUT Signal

This signal is available only as an output on the GPCTR0_OUT pin. GPCTR0_OUT reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This output is set to high-impedance at startup. Figure 4-31 shows the timing of GPCTR0_OUT.

Note When using external clocking mode with correlated DIO, this pin is used as an input for the external clock.

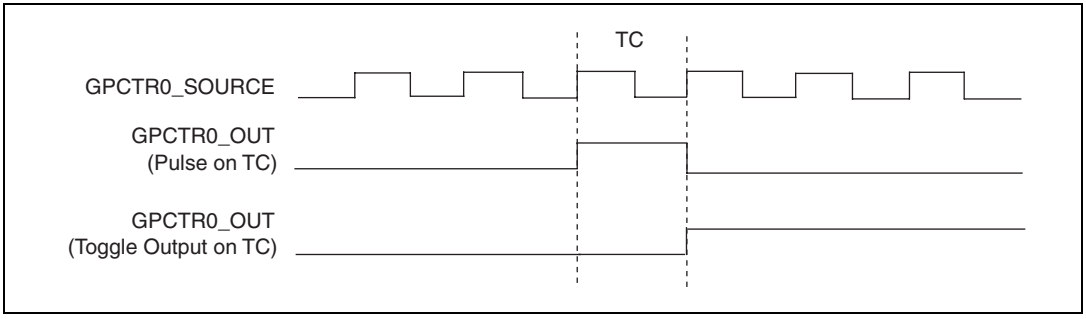


Figure 4-31. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 counts down when this pin is at a logic low and count up when it is at a logic high. You can disable this input so that software can control the up-down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, GPCTR1_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1, even if the source clock is being externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-32 shows the timing requirements for GPCTR1_SOURCE.

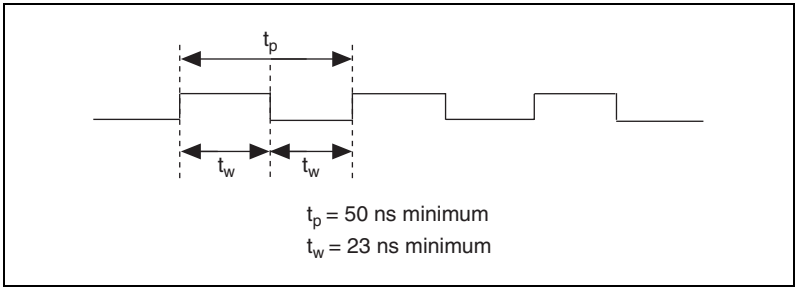


Figure 4-32. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates GPCTR1_SOURCE unless you select some external source.

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, GPCTR1_GATE is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform such actions as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, GPCTR1_GATE monitors the actual gate signal connected to general-purpose counter 1, even if the gate is being externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-33 shows the timing requirements for GPCTR1_GATE.

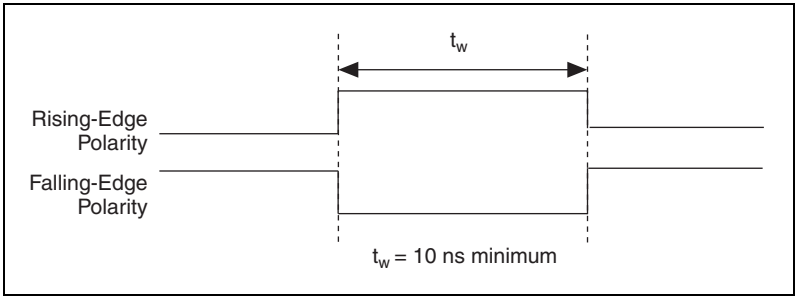


Figure 4-33. GPCTR1_GATE Signal Timing in Edge-Detection Mode

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. GPCTR1_OUT monitors the TC device general-purpose counter 1. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to high-impedance at startup.

Figure 4-34 shows the timing requirements for GPCTR1_OUT.

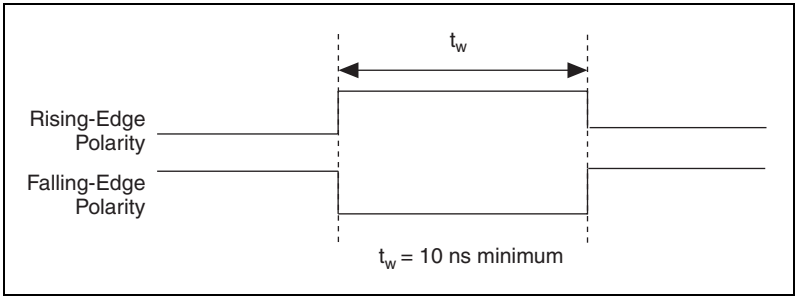
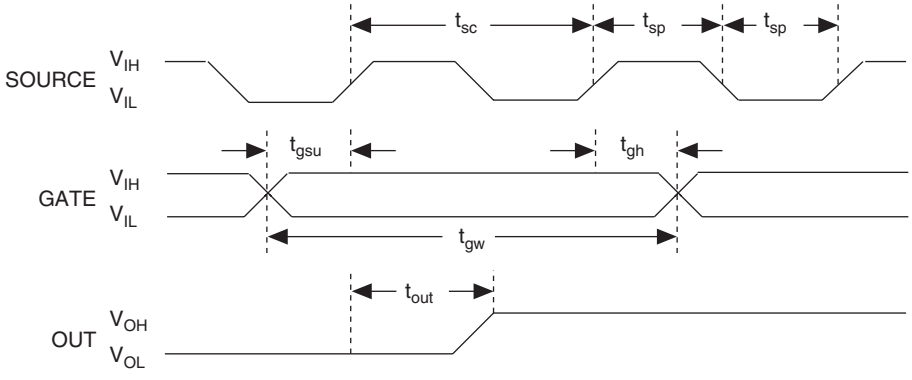


Figure 4-34. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that software can control the up-down functionality and leave the DIO7 pin free for general use. Figure 4-35 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals of the device.



Source Clock Period	t_{sc}	50 ns minimum
Source Pulse Width	t_{sp}	23 ns minimum
Gate Setup Time	t_{gsu}	10 ns minimum
Gate Hold Time	t_{gh}	0 ns minimum
Gate Pulse Width	t_{gw}	10 ns minimum
Output Delay Time	t_{out}	80 ns maximum

Figure 4-35. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-35 are referenced to the rising edge of the SOURCE signal. The assumption for this timing diagram is that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, would apply when the counter is programmed to count falling edges.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on the NI 6013/6014. Figure 4-35 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-35. The gate signal is not required to be held after the active edge of the source signal.

If you use an internal timebase clock, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the NI 6013/6014. Figure 4-35 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal is available only as an output on the FREQ_OUT pin. The device frequency generator outputs the FREQ_OUT pin. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software-selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software-selectable. This output is set to high-impedance at startup.

Field Wiring Considerations

Environmental noise can seriously affect the accuracy of measurements made with the device if you do not take proper care when running signal wires between signal sources and the device. The following recommendations apply mainly to AI signal routing to the device, although they also apply to signal routing in general.

Minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential AI connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect AI signals to the device. With this type of wire, the signals attached to the CH+ and CH– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a computer-based DAQ system is the video monitor. Separate the monitor from the analog signals as much as possible.
- Separate device signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the device signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.

- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

For more information, refer to the NI Developer Zone tutorial, *Field Wiring and Noise Consideration for Analog Signals*, at `ni.com/zone`.

5

Calibration

This chapter discusses the calibration procedures for the NI 6013/6014. NI-DAQ includes calibration functions for performing all of the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the NI 6013/6014, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of device calibration is required for most applications. If you do not calibrate the NI 6013/6014, the signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you and described in this chapter. The first level is the fastest, easiest, and least accurate, whereas the last level is the slowest, most difficult, and most accurate.

Loading Calibration Constants

The NI 6013/6014 is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the device is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ determines when loading calibration constants is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

In the EEPROM, there is a user-modifiable calibration area in addition to the permanent factory calibration area. The user-modifiable calibration area allows you to load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed. This method of calibration is not very accurate because it does not take into

account the fact that the device measurement and output voltage errors can vary with time and temperature. It is better to self-calibrate when the device is installed in the environment in which it is used.

Self-Calibration

The NI 6013/6014 can measure and correct for almost all of its calibration-related errors without any external signal connections. NI-DAQ provides a self-calibration method. This self-calibration process, which generally takes less than two minutes, is the preferred method of assuring accuracy in your application. Initiate self-calibration to minimize the effects of any offset and gain drifts, particularly those due to warmup.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the following section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

External Calibration

The NI 6013/6014 has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using the device at an extreme temperature or if the onboard reference has not been measured for a year or more, you may wish to externally calibrate the device.

An external calibration refers to calibrating the device with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process and the results can be saved in the EEPROM, so you should not have to perform an external calibration very often. You can externally calibrate the device by calling the NI-DAQ calibration function.

To externally calibrate the device, be sure to use a very accurate external reference. The reference should be several times more accurate than the device itself.

A

Specifications

This appendix lists the specifications of the NI 6013/6014.
These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels ..... 16 single-ended or 8 differential (software-selectable per channel)

Type of ADC..... Successive approximation

Resolution ..... 16 bits, 1 in 65,536

Sampling rate ..... 200 kS/s guaranteed

Input signal ranges ..... Bipolar only

Device Gain (Software-Selectable)	Range
0.5	±10 V
1	±5 V
10	±500 mV
100	±50 mV

Input coupling ..... DC

Overvoltage protection

Signal Name	Powered Off	Powered On
ACH<0..15>	±15 V	±25 V
AISENSE	±15 V	±25 V

FIFO buffer size.....512 samples

Data transfers.....DMA, interrupts, programmed I/O

DMA modes.....Scatter-gather (Single transfer, demand transfer)

Number of DMA channels.....1[1]

Configuration memory size.....512 words

Accuracy Information

Nominal Range at Full Scale (V)	Absolute Accuracy							Relative Accuracy	
	% of Reading		Offset	Noise + Quantization (µV)		Absolute Accuracy at Full Scale (mV)	Temp Drift	Resolution (µV)	
	24 Hours	1 Year	(µV)	Single Pt.	Averaged		(%/°C)	Single Point	Averaged
±10	0.0658	0.0700	1897.5	933.0	82.40	8.984	0.0010	1084.90	108.49
±5	0.0158	0.0200	959.8	466.5	41.20	2.003	0.0005	542.45	54.245
±0.5	0.0658	0.0700	115.8	56.2	5.035	0.471	0.0010	66.299	6.630
±0.05	0.0658	0.0700	31.4	31.40	3.067	0.069	0.0010	40.382	4.038

Note: Accuracies are valid for measurements after calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings. Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory calibration temperature.

Transfer Characteristics

Relative accuracy.....±1.0 LSB typ, ±3.0 LSB max

DNL.....±0.5 LSB typ, ±1.0 LSB max

No missing codes.....16 bits, guaranteed

Offset error

Pregain error after calibration.....±2.0 µV max

Pregain error before calibration.....±28.8 mV max

Postgain error after calibration.....±305 µV max

Postgain error before calibration.....±40.2 mV max

[1] The NI 6013/6014 has one DMA channel to be shared by all resources on the device.

Gain error (relative to calibration reference)

After calibration (gain = 1) ..... ±74 ppm of reading max

Before calibration ..... ±18,900 ppm of reading max

Gain ≠ 1 with gain error adjusted to 0 at gain = 1 ..... ±300 ppm of reading max

Amplifier Characteristics

Input impedance

Normal powered on ..... 100 GΩ in parallel with 100 pF

Powered off..... 820 Ω

Overload..... 820 Ω

Input bias current ..... ±200 pA

Input offset current..... ±100 pA

CMRR (DC to 60 Hz)

Gain 0.5, 1.0..... 85 dB

Gain 10, 100..... 96 dB

Dynamic Characteristics

Bandwidth

Signal	Bandwidth
Small (–3 dB)	425 kHz
Large (1% THD)	450 kHz

Settling time for full-scale step

Gain 100..... ±2 LSB, 5 µs typ

Gain 1, 10..... ±2 LSB, 5 µs max

Gain 0.5..... ±4 LSB, 5 µs typ

System noise ($LSB_{rms,}$ including quantization)

Gain	LSB_{rms}
0.5, 1.0	0.9
10	1.1
100	6.7

Crosstalk .....DC to 100 kHz
Adjacent channels.....–75 dB
Other channels .....≤ –90 dB

Stability

Recommended warm-up time.....15 min

Offset temperature coefficient
Pregain.....±20 µV/°C
Postgain .....±175 µV/°C

Gain temperature coefficient .....±32 ppm/°C

Analog Output

- NI 6014 only

Output Characteristics

Number of channels.....2 voltage

Resolution.....16 bits, 1 in 65,536

Max update rate
DMA.....10 kHz, system dependent
Interrupts.....1 kHz, system dependent

Type of DAC .....Double buffered, multiplying

FIFO buffer size.....None

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Scatter-gather (Single transfer, demand transfer)

Number of DMA channels .....1[1]

[1] The NI 6013/6014 has one DMA channel to be shared by all resources on the device.

Accuracy Information

Nominal Range (V)		Absolute Accuracy					
		% of Reading			Offset (µV)	Temp Drift (%/°C)	Absolute Accuracy at Full Scale (µV)
Positive FS	Negative FS	24 Hours	90 Days	1 Year			
10	–10	0.0154	0.0174	0.0196	1,873	0.0005	3,835

Transfer Characteristics

Relative accuracy (INL)..... ±3 LSB, typ

DNL ..... ±2 LSB, typ

Monotonicity..... 15 bits

Offset error

After calibration..... ±372 µV max

Before calibration ..... ±250 mV max

Gain error (relative to internal reference)

After calibration..... ±75 ppm

Before calibration ..... ±22,700 ppm

Voltage Output

Range ..... ±10 V

Output coupling..... DC

Output impedance ..... 0.1 Ω max

Current drive ..... ±5 mA max

Protection ..... Short-circuit to ground

Power-on state (steady state)..... ±250 mV

Initial power-up glitch

Magnitude ..... ±6.0 V

Duration ..... 4 ms

Power reset glitch

Magnitude.....±3.0 V

Duration.....3 ms

Dynamic Characteristics

Settling time for full-scale step.....8 µs to ±1 LSB accuracy

Slew rate .....4 V/µs

Noise.....360 μV_{rms}, DC to 400 kHz

Midscale transition glitch

Magnitude.....±200 mV

Duration.....2.0 µs

Stability

Offset temperature coefficient .....±128 µV/°C

Gain temperature coefficient .....±26.8 ppm/°C

Digital I/O

Number of channels.....8 input/output

Compatibility .....TTL/CMOS

DIO<0..7>

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 10 mA)	4.35 V	—

Power-on state ..... Input (high-impedance), 1.5 kΩ pull down to DGND

Data transfers ..... Programmed I/O

Max transfer rate ..... 50 kwords/s, system dependent

Timing I/O

Number of channels ..... 2 up/down counter/timers, 1 frequency scaler

Resolution

- Counter/timers ..... 24 bits
- Frequency scalers ..... 4 bits

Compatibility ..... TTL/CMOS

Base clocks available

- Counter/timers ..... 20 MHz, 100 kHz
- Frequency scalers ..... 10 MHz, 100 kHz

Base clock accuracy ..... ±0.01%

Max source frequency ..... 20 MHz

Min source pulse duration ..... 10 ns in edge-detect mode

Min gate pulse duration ..... 10 ns in edge-detect mode

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Scatter-gather (Single transfer, demand transfer)

Number of DMA channels ..... 1[1]

[1] The NI 6013/6014 has one DMA channel to be shared by all resources on the device.

Triggers

Digital Trigger

Compatibility ..... TTL

Response ..... Rising or falling edge

Pulse width ..... 10 ns min

Calibration

Recommended warm-up time ..... 15 min

Interval ..... 1 year

External calibration reference ..... >6 and <10 V

Onboard calibration reference

Level ..... 5.000 V (±3.5 mV)
(over full operating temperature, actual value stored in EEPROM)

Temperature coefficient ..... ±5 ppm/°C max

Long-term stability ..... ±15 ppm/$\sqrt{1{,}000\ \text{h}}$

Power Requirement

+5 VDC (±5%) ..... 0.7 A

Note Excludes power consumed through V_{CC} available at the I/O connector.

Power available at I/O connector ..... +4.65 to +5.25 VDC at 1 A

Physical

Dimensions
(not including connectors) ..... 17.5 by 10.6 cm (6.9 by 4.2 in.)

I/O connector ..... 68-pin male SCSI-II type

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth..... ±11 V, Installation Category II

Environmental

Operating temperature..... 0 to 50 °C

Storage temperature ..... –20 to 70 °C

Humidity ..... 10 to 70% RH, noncondensing

Maximum altitude ..... 2,000 meters

Pollution Degree (indoor use only)..... 2

Safety

The NI 6013/6014 meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- EN 61010-1:1993/A2:1995, IEC 61010-1:1990/A2:1995
- UL 3101-1:1993, UL 3111-1:1994, UL 3121:1998
- CAN/CSA c22.2 no. 1010.1:1992/A2:1997

Electromagnetic Compatibility

CE, C-Tick, and FCC Part 15 (Class A) Compliant

Electrical emissions..... EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Electrical immunity..... Evaluated to EN 61326:1998, Table 1

Note For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the DoC for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by the product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

B

Custom Cabling and Optional Connectors

This appendix describes the various cabling and connector options for the NI 6013/6014.

Custom Cabling

NI offers cables and accessories for you to prototype your application or to use if you frequently change device interconnections.

If you want to develop your own cable, however, adhere to the following guidelines for best results:

- For AI signals, use shielded twisted-pair wires for each AI pair for differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a backshell kit for making custom 68-pin cables are available from NI.

The parts in the following list are recommended for connectors that mate to the I/O connector on the NI 6013/6014:

- Honda 68-position, solder cup, female connector
- Honda backshell

Optional Connectors

Figure B-1 shows the pin assignments for the 68-pin connector. This connector is available when you use the SH6868 or R6868 cable assemblies.

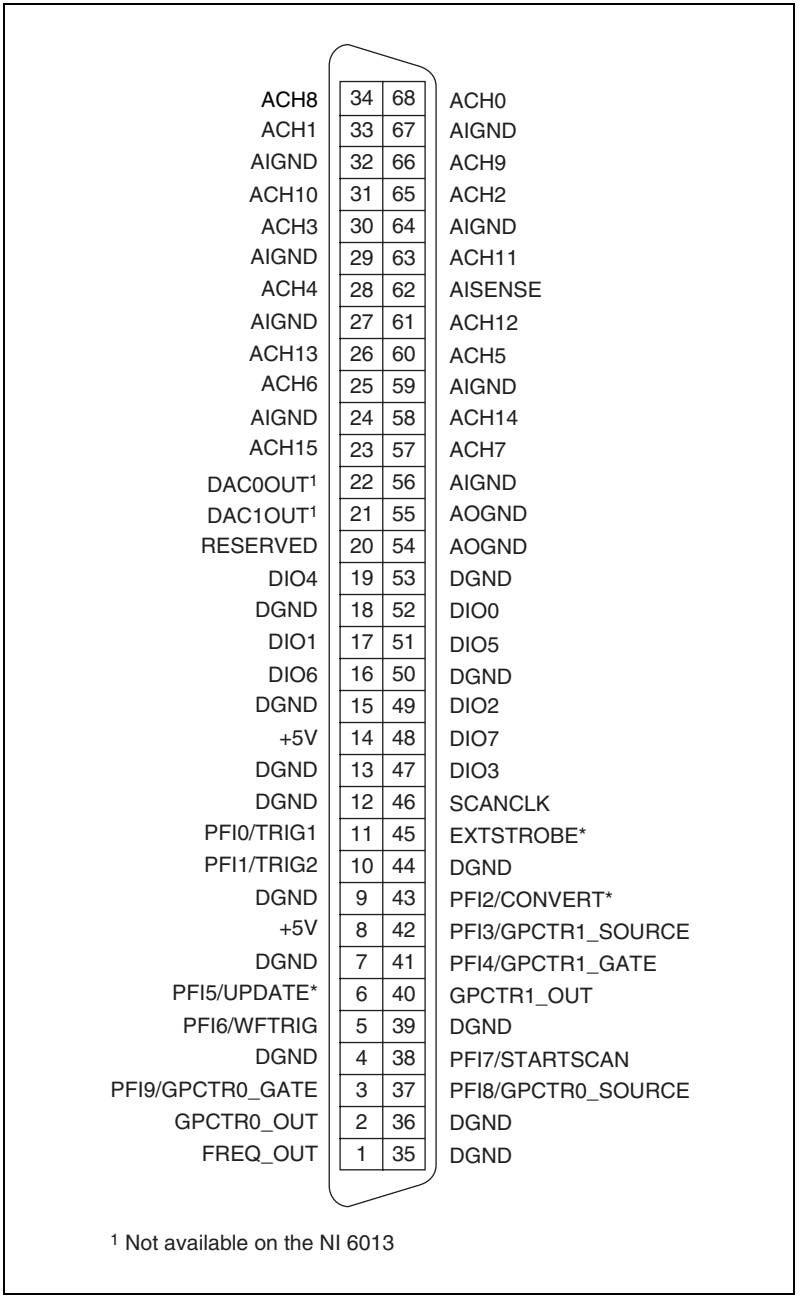

ACH8 34 68 ACH0
ACH1 33 67 AIGND
AIGND 32 66 ACH9
ACH10 31 65 ACH2
ACH3 30 64 AIGND
AIGND 29 63 ACH11
ACH4 28 62 AISENSE
AIGND 27 61 ACH12
ACH13 26 60 ACH5
ACH6 25 59 AIGND
AIGND 24 58 ACH14
ACH15 23 57 ACH7
DAC0OUT1 22 56 AIGND
DAC1OUT1 21 55 AOGND
RESERVED 20 54 AOGND
DIO4 19 53 DGND
DGND 18 52 DIO0
DIO1 17 51 DIO5
DIO6 16 50 DGND
DGND 15 49 DIO2
+5V 14 48 DIO7
DGND 13 47 DIO3
DGND 12 46 SCANCLK
PFI0/TRIG1 11 45 EXTSTROBE*
PFI1/TRIG2 10 44 DGND
DGND 9 43 PFI2/CONVERT*
+5V 8 42 PFI3/GPCTR1_SOURCE
DGND 7 41 PFI4/GPCTR1_GATE
PFI5/UPDATE* 6 40 GPCTR1_OUT
PFI6/WFTRIG 5 39 DGND
DGND 4 38 PFI7/STARTSCAN
PFI9/GPCTR0_GATE 3 37 PFI8/GPCTR0_SOURCE
GPCTR0_OUT 2 36 DGND
FREQ_OUT 1 35 DGND
1 Not available on the NI 6013

Figure B-1. 68-Pin Connector Pin Assignments

Figure B-2 shows the pin assignments for the 50-pin connector. This connector is available when you use the SH6850 or R6850 cable assemblies.

AIGND	1	2	AIGND
ACH0	3	4	ACH8
ACH1	5	6	ACH9
ACH2	7	8	ACH10
ACH3	9	10	ACH11
ACH4	11	12	ACH12
ACH5	13	14	ACH13
ACH6	15	16	ACH14
ACH7	17	18	ACH15
AISENSE	19	20	DAC0OUT[1]
DAC1OUT[1]	21	22	RESERVED
AOGND	23	24	DGND
DIO0	25	26	DIO4
DIO1	27	28	DIO5
DIO2	29	30	DIO6
DIO3	31	32	DIO7
DGND	33	34	+5V
+5V	35	36	SCANCLK
EXTSTROBE*	37	38	PFI0/TRIG1
PFI1/TRIG2	39	40	PFI2/CONVERT*
PFI3/GPCTR1_SOURCE	41	42	PFI4/GPCTR1_GATE
GPCTR1_OUT	43	44	PFI5/UPDATE*
PFI6/WFTRIG	45	46	PFI7/STARTSCAN
PFI8/GPCTR0_SOURCE	47	48	PFI9/GPCTR0_GATE
GPCTR0_OUT	49	50	FREQ_OUT

[1] Not available on the NI 6013

Figure B-2. 50-Pin Connector Pin Assignments

C

Common Questions

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of the NI 6013/6014.

General Information

What is the DAQ-STC?

The DAQ-STC is the system timing control application-specific integrated circuit (ASIC) designed by NI and is the backbone of the NI 6013/6014. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into the following three groups:

- AI—two 24-bit, two 16-bit counters
- AO—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be configured independently with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities such as buffered pulse generation, equivalent time sampling, and seamless changing of the sampling rate are possible.

What does sampling rate mean to me?

Sampling rate is the fastest you can acquire data on the NI 6013/6014 and still achieve accurate results. For example, these devices have a sampling rate of 200 kS/s. This sampling rate is aggregate: one channel at 200 kS/s or two channels at 100 kS/s per channel illustrates the relationship.

What type of 5 V protection does the NI 6013/6014 have?

The NI 6013/6014 has 5 V lines equipped with a self-resetting 1 A fuse.

How do I use the NI 6013/6014 with the C API in NI-DAQ?

The *NI-DAQ User Manual for PC Compatibles* contains example code and describes the general programming flow when using the NI-DAQ C API. For a list of functions that support the NI 6013/6014, refer to the *NI-DAQ Function Reference Help* (NI-DAQ version 6.7 or later) or the *NI-DAQ Function Reference Manual for PC Compatibles* (NI-DAQ version 6.6 or earlier).

Refer to `ni.com/manuals` for the *NI-DAQ User Manual for PC Compatibles*, and refer to `ni.com/downloads` to download the version of NI-DAQ that your application requires.

Installing and Configuring the Device

How do I set the base address for the NI 6013/6014?

The base address of the NI 6013/6014 is assigned automatically through the PCI bus protocol. This assignment is completely transparent to you.

What jumpers should I be aware of when configuring the NI 6013/6014?

The NI 6013/6014 is jumperless and switchless.

Which NI document should I read first to get started using DAQ software?

The *DAQ Quick Start Guide* and the NI-DAQ or ADE release notes documentation are good places to start.

What version of NI-DAQ must I have to use the NI 6013/6014?

The NI 6013/6014 requires NI-DAQ version 6.9.3 or later.

What is the best way to test the NI 6013/6014 without programming the device?

If you are using Windows, Measurement & Automation Explorer (MAX) has a Test Panel option that is available by selecting **Devices and Interfaces** and then selecting the device. The Test Panels are excellent tools for performing simple functional tests of the device, such as AI, DIO, and counter/timer tests.

Analog Input and Output

I am using the device in differential AI mode, and I have connected a differential input signal, but the readings are random and drift rapidly. What is wrong?

Check the ground reference connections. The signal may be referenced to a level that is considered *floating* with reference to the device ground reference. Even if you are in differential mode, the signal *must* still be referenced to the same ground level as the device reference. You can use one of various methods to achieve ground reference while maintaining a high common-mode rejection ratio (CMRR). Refer to Chapter 4, *Connecting Signals*, for more information.

I am using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When it switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of the output signal.

Can I programmatically enable channels on the NI 6013/6014 to acquire in different modes? For example, can I configure ACH0 in DIFF input mode and ACH1 in NRSE input mode?

Channels on the NI 6013/6014 can be enabled to acquire in different modes, but different pairs of channels are used in different modes. In the example configuration given above, ACH0 and ACH8 are configured in DIFF mode and ACH1 and AISENSE are configured in NRSE mode. In this configuration, ACH8 is not used in a single-ended configuration. To enable multimode scanning in LabVIEW, use the coupling and input configuration cluster input of the AI Config VI. This input has a one-to-one correspondence with the channel array input of the AI Config VI. You must list all channels either individually or in groups of channels with the same input configuration. For example, if you want ACH0 to be differential, and ACH1 and ACH2 to be NRSE, Figure C-1 demonstrates how to program this configuration in LabVIEW.

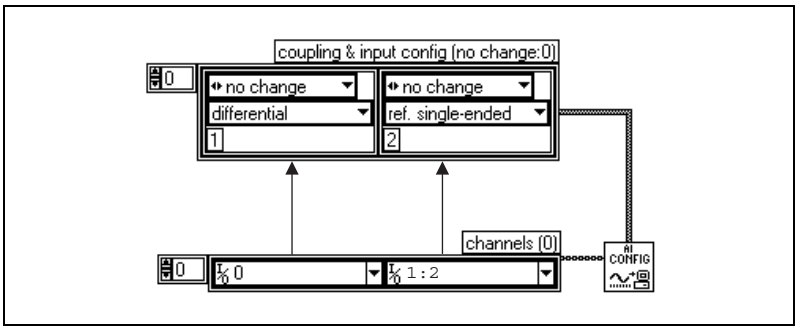


Figure C-1. Configuring Channels to Acquire in Different Modes in LabVIEW

To enable multimode scanning in using NI-DAQ functions, call the AI_Configure function for each channel.

I am seeing crosstalk or ghost voltages when sampling multiple channels. What does this mean?

You maybe experiencing a phenomenon called *charge injection*, which occurs when you sample a series of high-output impedance sources with a multiplexer. Multiplexers contain switches, usually made of switched capacitors. When a channel, for example ACH0, is selected in a multiplexer, those capacitors accumulate charge. When the next channel, for example ACH1, is selected, the accumulated current, or charge, leaks backward through that channel. If the output impedance of the source connected to ACH1 is high enough, the resulting reading can somewhat reflect the voltage trends in ACH0. To circumvent this problem, you must use a voltage follower that has operational amplifiers (op-amps) with unity gain for each high-impedance source before connecting to the DAQ device. Otherwise, you must decrease the rate at which each channel is sampled.

Another common cause of channel crosstalk is due to sampling among multiple channels at various gains. In this situation, the settling times may increase. For more information on charge injection and sampling channels at different gains, refer to the *Multichannel Scanning Considerations* section of Chapter 3, *Hardware Overview.*

How can I use the STARTSCAN and CONVERT* signals on the NI 6013/6014 to sample the AI channel(s)?

The NI 6013/6014 uses the STARTSCAN and CONVERT* signals to perform interval sampling. As Figure C-2 shows, STARTSCAN controls the scan interval, which is determined by the following equality:

$$\frac{1}{scan\ interval} = scan\ rate$$

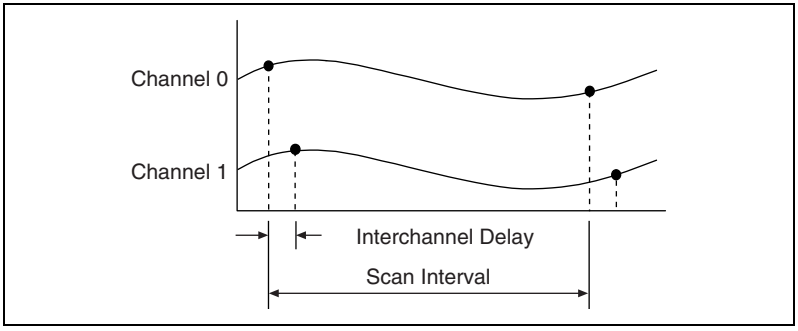


Figure C-2. Scan Interval

CONVERT* controls the interchannel delay, which is determined by the following equality:

$$\frac{1}{interchannel\ delay} = sampling\ rate$$

This method allows multiple channels to be sampled relatively quickly in relationship to the overall scan rate, providing a nearly simultaneous effect with a fixed delay between channels.

Timing and Digital I/O

What types of triggering can be hardware-implemented on the NI 6013/6014?

Digital triggering is hardware-supported on the NI 6013/6014.

I am using one of the general-purpose counter/timers on the device, but I do not see the counter/timer output on the I/O connector. Why?

If you are using the NI-DAQ language interface or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` function in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are tri-stated.

What are the PFIs and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

If you are using NI-DAQ or Measurement Studio, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use the AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, and Counter Set Attribute advanced-level VIs to indicate which function the connected signal serves. Use the Route Signal VI to enable the PFI lines to output internal signals.

Caution If you enable a PFI line for output, do *not* connect any external signal sources to it; if you do, you can damage the device, the computer, and the connected equipment.

Table C-1 corresponds the hardware signal names to the software signal names in LabVIEW and NI-DAQ.

Table C-1. Signal Name Equivalencies

Hardware Signal Name	LabVIEW Route Signal	NI-DAQ Select_Signal
TRIG1	AI Start Trigger	ND_IN_START_TRIGGER
TRIG2	AI Stop Trigger	ND_IN_STOP_TRIGGER
STARTSCAN	AI Scan Start	ND_IN_SCAN_START
SISOURCE	—	ND_IN_SCAN_CLOCK_TIMEBASE
CONVERT*	AI Convert	ND_IN_CONVERT
AIGATE	—	ND_IN_EXTERNAL_GATE
WFTRIG	AO Start Trigger	ND_OUT_START_TRIGGER
UPDATE*	AO Update	ND_OUT_UPDATE
UISOURCE	—	ND_OUT_UPDATE_CLOCK_TIMEBASE
AOGATE	—	ND_OUT_EXTERNAL_GATE

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high-impedance by the hardware. This setting means that the device circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in Table 4-3, *I/O Signal Summary for the NI 6013/6014*. These resistors weakly pull the output to either a logic-high or logic-low state. For example, DIO<0> is in the high-impedance state after power on, and Table 4-3, *I/O Signal Summary for the NI 6013/6014*, shows the 1.5 kΩ pull-down resistor. This pull-down resistor sets the DIO<0> pin to a logic low when the output is in a high-impedance state.

D

Technical Support and Professional Services

Visit the following sections of the NI Web site at ni.com for technical support and professional services:

- **Support**—Online technical support resources include the following:
  - **Self-Help Resources**—For immediate answers and solutions, visit our extensive library of technical support resources available in English, Japanese, and Spanish at ni.com/support. These resources are available for most products at no cost to registered users and include software drivers and updates, a KnowledgeBase, product manuals, step-by-step troubleshooting wizards, hardware schematics and conformity documentation, example code, tutorials and application notes, instrument drivers, discussion forums, a measurement glossary, and so on.
  - **Assisted Support Options**—Contact NI engineers and other measurement and automation professionals by visiting ni.com/ask. Our online system helps you define your question and connects you to the experts by phone, discussion forum, or email.
- **Training**—Visit ni.com/custed for self-paced tutorials, videos, and interactive CDs. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, NI Alliance Program members can help. To learn more, call your local NI office or visit ni.com/alliance.

If you searched ni.com and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

Glossary

Prefix	Meanings	Value
p-	pico	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Symbols

%	percent
+	positive of, or plus
–	negative of, or minus
±	plus or minus
/	per
°	degree
Ω	ohm

A

A	amperes
A/D	analog-to-digital
ACH	AI channel signal

ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
AI	analog input
AIGATE	AI gate signal
AIGND	AI ground signal
AISENSE	AI sense signal
ANSI	American National Standards Institute
AO	analog output
AOGND	AO ground signal

B

base address	a memory address that serves as the starting address for programmable registers. All other addresses are located by adding to the base address.
bipolar	a signal range that includes both positive and negative values (for example, –5 to +5 V)
BC	buffered counter
bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the ISA and PCI bus.

C

C	Celsius
CalDAC	calibration DAC
CH	channel—pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.

CMRR	common-mode rejection ratio—a measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB)
common-mode signal	any voltage present at the instrumentation amplifier inputs with respect to amplifier ground
CONVERT*	convert signal
counter/timer	a circuit that counts external pulses or clock pulses (timing)

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
DAC0OUT	analog channel 0 output signal
DAC1OUT	analog channel 1 output signal
DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20log10 V1/V2, for signals in volts
DC	direct current
DGND	digital ground signal
DIFF	differential mode
differential input	an analog input consisting of two terminals, both of which are isolated from computer ground, whose difference is measured
DIO	digital input/output

dithering	the addition of Gaussian noise to an AI signal
DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	differential nonlinearity—a measure in least significant bit of the worst-case deviation of code widths from their ideal value of 1 LSB
DO	digital output
DoC	Declaration of Conformity
DOC	Department of Communications
driver	software that controls a specific hardware device such as a DAQ device or a GPIB interface board

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
EXTSTROBE	external strobe signal

F

FCC	Federal Communications Commission
FIFO	first-in first-out memory buffer—the first data stored is the first data sent to the acceptor. FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be retrieved or output. For example, an AI FIFO stores the results of A/D conversions until the data can be retrieved into system memory, a process that requires the servicing of interrupts and often the programming of the DMA controller. This process can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored on the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.

floating signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called nonreferenced signal sources. Some common example of floating signal sources are batteries, transformers, or thermocouples.
FREQ_OUT	frequency output signal

G

gain	the factor by which a signal is amplified, sometimes expressed in decibels
gain accuracy	a measure of deviation of the gain of an amplifier from the ideal gain
GATE	gate signal
glitch	an unwanted momentary deviation from a desired signal
GPCTR	general purpose counter
GPCTR0_GATE	general purpose counter 0 gate signal
GPCTR0_OUT	general purpose counter 0 output signal
GPCTR0_SOURCE	general purpose counter 0 clock source signal
GPCTR0_UP_DOWN	general purpose counter 0 up down
GPCTR1_GATE	general purpose counter 1 gate signal
GPCTR1_OUT	general purpose counter 1 output signal
GPCTR1_SOURCE	general purpose counter 1 clock source signal
GPCTR1_UP_DOWN	general purpose counter 1 up down
grounded measurement system	*See* referenced single-ended configuration.

H

h	hour
Hz	hertz—the number of scans read or updates written per second

I

I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
in.	inches
INL	integral nonlinearity—a measure in LSB of the worst-case deviation from the ideal A/D or D/A transfer characteristic of the analog I/O circuitry
input bias current	the current that flows into the inputs of a circuit
input impedance	the resistance and capacitance between the input terminals of a circuit
input offset current	the difference in the input bias currents of the two inputs of an instrumentation amplifier
instrumentation amplifier	a circuit whose output voltage with respect to ground is proportional to the difference between the voltages at its two high impedance inputs
interrupt	a computer signal indicating that the CPU should suspend its current task to service a designated activity
I_{OH}	current, output high
I_{OL}	current, output low

K

k	kilo—the standard metric prefix for 1,000, or 10^3, used with units of measure such as volts, hertz, and meters
kS	1,000 samples

L

LabVIEW	Laboratory Virtual Instrument Engineering Workbench—a program development application based on the programming language G and used commonly for test and measurement purposes
LED	light-emitting diode

library	a file containing compiled object modules, each comprised of one of more functions, that can be linked to other object modules that make use of these functions. `NIDAQMSC.LIB` is a library that contains NI-DAQ functions. The NI-DAQ function set is broken down into object modules so that only the object modules that are relevant to your application are linked in, while those object modules that are not relevant are not linked.
linearity	the adherence of device response to the equation $R = KS$, where R = response, S = stimulus, and K = a constant
LSB	least significant bit

M

MITE	MXI Interface to Everything—a custom ASIC designed by NI that implements the PCI bus interface. The MITE supports bus mastering for high-speed data transfers over the PCI bus.
MSB	most significant bit
mux	multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single AI channel

N

NI	National Instruments
NI-DAQ	National Instruments driver software for DAQ hardware
noise	an undesirable electrical signal—noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
NRSE	nonreferenced single-ended mode—all measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground.

O

OUT	output pin—a counter output pin where the counter can generate various TTL pulse waveforms

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
pd	pull down
PFI	programmable function input
PFI0/TRIG1	PFI0/trigger 1
PFI1/TRIG2	PFI1/trigger 2
PFI2/CONVERT*	PFI2/convert
PFI3/GPCTR1_ SOURCE	PFI3/general purpose counter 1 source
PFI4/GPCTR1_GATE	PFI4/general purpose counter 1 gate
PFI5/UPDATE*	PFI5/update
PFI6/WFTRIG	PFI6/waveform trigger
PFI7/STARTSCAN	PFI7/start of scan
PFI8/GPCTR0_ SOURCE	PFI8/general purpose counter 0 source
PFI9/GPCTR0_GATE	PFI9/general purpose counter 0 gate
PGIA	programmable gain instrumentation amplifier
port	(1) a communications connection on a computer or a remote controller; (2) a digital port, consisting of four or eight lines of digital input and/or output

ppm	parts per million
pu	pull up

Q

quantization error	the inherent uncertainty in digitizing an analog value due to the finite resolution of the conversion process

R

referenced single-ended configuration	RSE—all measurements are made with respect to a common reference measurement system or ground; also called a grounded measurement system
relative accuracy	a measure in LSB of the accuracy of an ADC. It includes all non-linearity and quantization errors. It does not include offset and gain errors of the circuitry feeding the ADC.
resolution	the smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244% of full scale.
ribbon cable	a flat cable in which the wires are lined up, not bunched together
rms	root mean square—the square root of the average value of the square of the instantaneous signal amplitude; a measure of signal amplitude
RSE	*See* referenced single-ended configuration.

S

s	seconds
S	samples
S/s	samples per second—used to express the rate at which a DAQ device samples an analog signal
sample counter	the clock that counts the output of the channel clock, in other words, the number of samples taken. On devices with simultaneous sampling, this counter counts the output of the scan clock and hence the number of scans.

SC	scan counter
scan	one or more analog or digital input samples. Typically, the number of input samples in a scan is equal to the number of channels in the input group. For example, one pulse from the scan clock produces one scan which acquires one new sample from every AI channel in the group.
scan clock	the clock controlling the time interval between scans
settling time	the amount of time required for a voltage to reach its final value within specified limits
SI	scan interval
SI2	sample interval
signal conditioning	the manipulation of signals to prepare them for digitizing
SISOURCE	SI counter clock signal
software trigger	a programmed event that triggers an event such as data acquisition
SOURCE	source signal
STARTSCAN	start scan signal
STC	system timing controller

T

TC	terminal count—the highest value of a counter
t_{gh}	gate hold time
t_{gsu}	gate setup time
t_{gw}	gate pulse width
THD	total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibel or a percentage
t_{off}	pulse off
t_{out}	output delay time

t_p	pulse period
TRIG	trigger signal
trigger	any event that causes or starts some form of data capture
t_{sc}	source clock period
t_{sp}	source pulse width
TTL	transistor-transistor logic—a digital circuit composed of bipolar transistors wired in a certain manner
t_w	pulse width
two's complement	given a number *x* expressed in base 2 with *n* digits to the left of the radix point, the (base 2) number $2n - x$

U

UI	update interval
UISOURCE	update interval counter clock signal
update	the output equivalent of a scan. One or more analog or digital output samples. Typically, the number of output samples in an update is equal to the number of channels in the output group. For example, one pulse from the update clock produces one update which sends one new sample to every AO channel in the group.
update rate	the number of output updates per second

V

V	volts
V_{CC}	positive supply voltage
VDC	volts direct current
V_{IH}	volts, input high
V_{IL}	volts, input low

V_{in}	volts in
V_m	measured voltage
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{rms}	volts, root mean square

W

waveform	multiple voltage readings taken at a specific sampling rate
WFTRIG	waveform generation trigger signal
working voltage	the highest voltage that should be applied to a product in normal use, normally well under the breakdown voltage for safety margin.

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